*Total No. of Questions :10]* *[Total No. of Printed Pages :2*

**Roll No**.....

# EC-802

## B.E. VIII Semester

Examination June, 2013

## CMOS Circuit Design

***Time : Three Hours***

***Maximum Marks : 100*** ***Minimum Pass Marks :35***

*Note :* Attempt one question from each unit. All questions carry equal marks.

### Unit-I

I. a) Design the CMOS source follower and explain its working.

b) Discuss the frequency response of cascade stage amplifier.

OR

II. a) Design the CMOS cascade stage amplifier and explain its working.

b) Discuss the frequency response of differential pair amplifier.

### Unit-II

III. a) Explain the working of differential pair with MOS Loads.

b) Discuss the effect of feedback on noise.

OR

IV a) Discuss the different topologies of feedback.

b) Explain the working of switched capacitor amplifier and switched capacitor integrator.

## Unit-III

V. a) Explain with the help of circuit diagram explain the working of voltage controlled oscillator.

b) Discuss the working of charge pump PLL's.

OR

VI. a) Explain the working of VCO's with the help of mathematical model.

b) What are the non ideal effects in PLL's.

## Unit-IV

VII. a) Design the R-S flip flop using CMOS technology

b) Discuss briefly about serial access memories.

OR

VIII. a) Design the JK flip flop using CMOS technology

b) Discuss briefly about content addressable memory.

## Unit-V

IX. Write short notes on the following:

a) Comparators

b) Parallel prefix computations

OR

X. Write short notes on the following:

a) One/Zero Detector

b) Counters

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