

Roll No

MCSE - 103**M.E./M.Tech., I Semester**

Examination, June 2016

Advanced Computer Architecture**Time : Three Hours****Maximum Marks : 70****Note :** Attempt any five questions. All questions carry equal marks.

1. a) Discuss the Flynn's classification scheme of computer architecture. 7
- b) Describe the following terminology associated with pipeline computers : 7
 - i) Simple cycle ii) greedy cycle
 - iii) Forbidden latency iv) Bottleneds
2. a) Describe the various shared memory multiprocessors. 7
- b) Consider the execution of a program of 15,00,000 instructions by a linear pipeline processor with a clock rate of 1000 MHz.
 - i) Calculate the speed up factor in using pipeline as compared with an equivalent non pipelined processor.
 - ii) What are the efficiency and though put of pipelined processor. 7
3. a) Explain the parallel bubble sort algorithm using interconnection network. Also gives its time complexity to sort the elements. 7
- b) Explain internal data forwarding and possible hazards between read and write operation with respects to mechanism for instruction pipeline. 7

4. a) Explain the following terminology associated with SIMD computers : 7
 - i) Lock-step operation
 - ii) Masking of processing elements
 - iii) Shuffle exchange functions
 - iv) Recalculating Networks
- b) Explain the difference among UMA, NUMA, COMA and NORMA architecture. 7
5. a) Explain the temporal locality, spatial locality and sequential locality associated with program/data access in a memory hierarchy. 7
- b) How can air-traffic simulation be done on a multicomputer system, using decomposition technique? 7
6. a) Explain multiprocessing in MIMD mode and multiprocessing in MPMD mode. 7
- b) Explain the parallel algorithm for array processors. 7
7. a) What is cache coherence? Explain the various protocols of cache coherence. 7
- b) What are the types of operating systems used for parallel processing? How they are different from the normal OS. 7
8. Write short notes on any three of the following : 14
 - a) Bitonic merge sort
 - b) Remote procedure call
 - c) Vector processor
 - d) Scheduling and local balancing in multiprocessor
 - e) Dynamic interconnections
