

Roll No. 0192EC12MT18

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MEDC - 104

M.E./M.Tech. I Semester

Examination, December 2012

VLSI Design

Time : Three Hours

Maximum Marks : 70

- Note : 1. Attempt all five questions.
2. Part-A is compulsory from each question.

1. a) Explain details of different aspects of digital CMOS circuit design.
- b) Discuss design abstraction and circuit validation with example.

OR

- c) What are the role of clean rooms in IC fabrication? Explain HERA filter used in clean rooms. Define class-1000 clean rooms.

2. a) Design the circuit described by the function $X = \overline{A(B+C)(D+E)}$ using CMOS logic. Also find the equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $\left(\frac{W}{L}\right) = 5$ for all

PMOS Transistor and $\left(\frac{W}{L}\right) = 2$ for all n MOS Transistors.

[2]

- b). Describe basic physical design and I/O structure.

OR

- 1 c) Discuss CMOS logic design rules and importance of power and delay in logic design.

3. a) Explain simulation and verification in system design with example.

- b) Discuss programmable gate array.

OR

- c) Describe procedure for CMOS chip design. Also draw flow diagram for the same.

4. a) How will you implement the ROM using subsystem design? Explain step by step?

- b) Discuss memory and control strategies. With suitable example.

OR

- c) Explain PLA and data operation in subsystem design.

5. a) Explain placement and Routing algorithms.

- b) What is CAD system? Explain logic synthesis and simulation.

OR

- c) Discuss layout and timing analysis.

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