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Roll No

MEMT - 104**M.E./M. Tech., I Semester**

Examination, December 2015

Advance Digital Circuit and PLC*Time : Three Hours**Max. Marks : 70*

- Note:** i) Attempt any two parts from each questions.
 ii) All questions carry equal marks.

1. a) Design a mod 5 counter using JK flip-flops.
 b) Explain the finite state machine concept with suitable example and diagram.
 c) Compare combinational and sequential circuits. Also explain representation of combinational circuit through VHDL.
2. a) Explain briefly about register-transfer level design.
 b) Explain the digital system implementation using algorithms state machine concepts.
 c) Explain what is the importance of the following terms in digital system implementation:
 i) Busing ii) Clocking and control

3. a) Give the PAL realization of the given function

$$\Omega(A, B, C, D, E, F) = \sum m(0, 2, 6, 7, 8, 12, 13)$$

$$x(A, B, C, D, E, F) = \sum m(0, 2, 6, 7, 8, 12, 13, 14)$$

$$y(A, B, C, D, E, F) = \sum m(2, 3, 8, 9, 10, 12, 13)$$

$$z(A, B, C, D, E, F) = \sum m(1, 3, 6, 9, 12, 4)$$

- b) Explain PLA and gate array with suitable examples.
- c) Discuss the PLA based control unit design.

4. a) Write a note on fault tolerance.
 b) Explain high speed computation hardware with suitable diagram.
 c) What is testing of a device? Describe testing of digital hardware design.
5. a) Give the application of PLC in control rooms of power plants.
 b) Implement a control panel for controlling a process plant using PLC in control room.
 c) Explain the working of micro programmed control unit.

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