Total No. of Questions :8] *[Total No. of Printed Pages :2*

Roll No .....

MEVD - 102

M.E./M.Tech., I Semester

Examination, December 2015

CMOS VLSI Design

Time : Three Hours

Maximum Marks :70

Note: i) Answer any five questions.
ii) All parts of each questions are to be attempted at one place.
iii) All the questions carry equal marks.

1. Explain VLSI design flow and explain the design concept of Hierarchy, Regularity, Modularity and Locality.

2. Draw complementary CMOS inverter DC characteristic and explain three region of operation of a CMOS inverter. Explain channel length modulation in MOS transistor.

3. Explain static and dynamic power dissipation in CMOS inverter. What is the significance of transistor sizing in any circuit design.

4. Write short note on layout design rule and explain latch-up in CMOS circuits.

5. Draw the circuit and layout of 4 × 1 MUX.

6. Design the circuit of 6T-SRAM and 3T-DRAM cell and explain its working in detail.

7. Write short note on FPGA and design the function
$F = xy + yz + xz$
using two input LUT.

8. Explain about CPLD and describe the difference between PAL and PLA with an example.

******