Roll No .....

MEVD - 102

M.E./M.Tech., I Semester

Examination, June 2013

CMOS VLSI Design

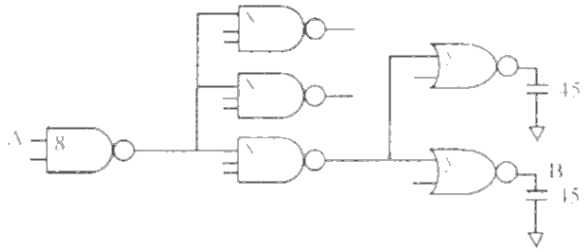
Time : Three Hours

Maximum Marks :70

Note: Attempt any five questions. All questions carry equal marks.

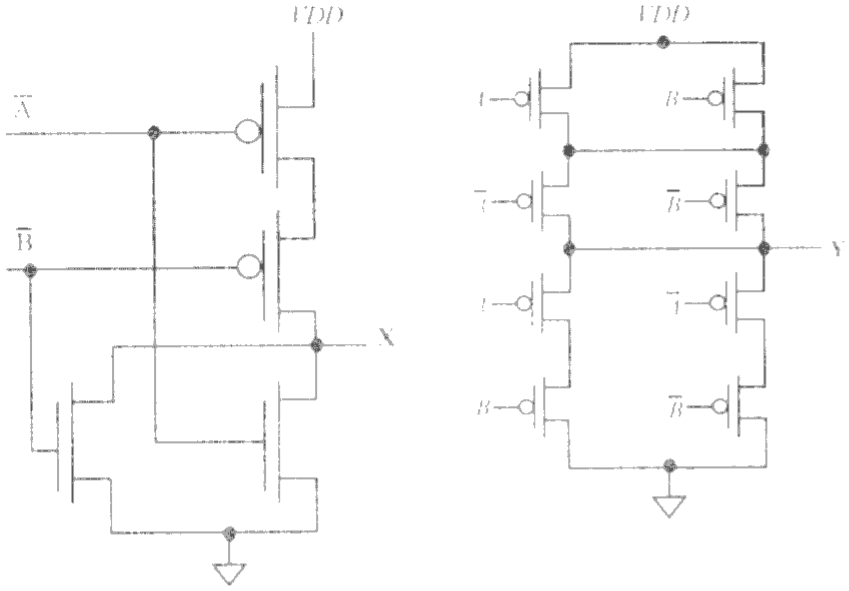
1. a) Compare the two technology scaling methods, namely the constant field scaling and constant power supply voltage scaling. Show analytically how the delay time, power dissipation, frequency of operation and power density are affected in terms of the scaling factor.

   b) Calculate the gate sizes x and y for least delay from A to B.



2. a) Explain the design hierarchies with example.

b) Identify the given logic circuit with A and B as input and give Boolean expression for X and Y.



a) Derive the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics.

b) Consider a CMOS inverter with the following parameters.

nMOS V_{Tn} = 0.6V, $\mu_n C_{ox}$ = 60 μA V^{-2}, $(W/L)_n$ = 8

pMOS V_{Tp} = -0.7V, $\mu_p C_{ox}$ = 25 μA V^{-2}, $(W/L)_p$ = 12 and V_{DD} = 3.3V

Calculate the Noise Margins and the Switching threshold (V_{th}) of the circuit.

a) Draw a 6 - T SRAM Cell and explain the Read and Write operations.

b) Realized the Boolean expression, Z = (D.E+A) · (B.C) + F using Standard CMOS and also find the equivalent CMOS inverter circuit, assuming that $(W/L)_p$ = 10 for all PMOS transistors and $(W/L)_n$ = 5 for all NMOS transistors.

5. a) Why is the packing density of MOS transistors more than that of bipolar transistors? What is Euler path in CMOS gates. Illustrate one layout involving Euler Path.

   b) Draw the stick Diagram for the given Boolean function and estimate its area.

   $OUT = \overline{D + A.(B+C)}$

6. a) Discuss the Charge Sharing problem in VLSI circuits. Explain various circuits for solving the Charge Sharing problem.

   b) Draw a transistor level two input NAND gate. Explain its sizing (a) considering V_{th} (b) for equal rise and fall times.

7. a) Draw Vds - Ids curve for a MOSFET. Now, show how this curve changes (a) with increasing Vgs (b) with increasing transistor width (c) considering Channel Length Modulation.

   b) Calculate Logical Effort for NAND Gate, NOR Gate, EX-OR Gate and EX-NOR Gate all with 3-input.

8. Write short notes on any four of the following:

   a) Sea of Gates

   b) CMOS Process Enhancements

   c) Latch up prevention techniques

   d) Non ideal conditions in MOS device model

   e) Various MOSFET Capacitances and their significance

   f) Set up time and hold time constraints

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