Total No. of Questions :8] *[Total No. of Printed Pages :2*

Roll No.....

MEVD-102

M.E/M.Tech. I Semester

Examination, June 2017

CMOS VLSI Design

Time : Three Hours

 Maximum Marks : 70

Note: i) Answer any five questions.
ii) All questions carry equal marks.
iii) Assume suitable data if required.

1. a) Draw and explain the graphical derivation of CMOS inverter characteristic.
   b) Draw and explain the CMOS inverter noise margin. Explain its characteristics.

2. a) Explain the second order effects. Draw and explain the sub threshold region.
   b) Write down different design rules for layout circuit.

3. a) Explain the parasitic effects in Integrated circuits.
   b) Derive an expression for channel resistance in voltage current characteristics of MOS transistor.

4. a) Explain the designing of ALU subsystem. What is its significances in a circuit? Explain with a suitable example.
   b) Give an introductory note on CAD tools. How this tool is beneficial for designing MOS circuits?

5. a) Draw and explain the accumulation, depletion and inversion function of V_{gs} in MOS capacitor characteristics.
   b) Give an introductory note on dynamic register element. Give its applications also.

6. a) Explain the concept of Power Dissipation. Explain the difference between static and dynamic dissipation. Derive its expressions.
   b) Discuss the designing of clocked sequential circuits. Explain the principle of two phase clocking. Explain it with a suitable example.

7. a) Is there any difference between the designing of PLA and PAL? Explain.
   b) Explain FPGA. Write its applications. What is the role of FPGA in field designing?

8. Explain the principle of Latch up. Discuss about its physical origin, its triggering and its prevention methods.

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