Total No. of Questions :8] *[Total No. of Printed Pages :2*

Roll No ...

MEVD - 103

M.E./M.Tech., I Semester

Examination, June 2014

Advanced Logic Design

Time : Three Hours

Maximum Marks : 70

Note : i) Attempt any five questions.
ii) All questions carry equal marks.

1. a) Give a brief over view of verilog.
   b) Design a CMOS NAND gate and discuss its working principle.

2. a) Explain briefly about the working of programmable logic devices.
   b) Realize Y = (A + C) (A + D) (A + B + C) using NOR gates. Explain the concept of bubble pushing.

3. a) Simplify the expression Y = Σm (3, 4, 5, 7, 9, 13, 14, 15) using k-map method and then implement the function using NAND gates.
   b) Give a brief overview of verilog data types and operators.

4. a) Write a verilog module for one bit full adder using built in verilog gates.
   b) How is behavioral modeling done in the verilog?

5. a) Give the verilog specifications for a 4:1 multiplexer.
   b) Design a verilog module for a D Latch.

6. a) Design a verilog module for a 4 bit up counter.
   b) Explain briefly about the working and classification of finite state machine.

7. a) Discuss the designing process of synchronous sequential circuits.
   b) Give a brief note on designing of skew finite state machine.

8. Write short notes on the following :
   a) Hazards and glitches.
   b) Metastability.
   c) Noise margins and fan out.

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