Roll No .....

MEVD - 104

M.E./M.Tech. I Semester

Examination, June 2013

Digital Signal Processing

Time : Three Hours

Maximum Marks : 70

Note : 1. *Attempt any five questions.*
2. *All questions carry equal marks.*

1. a) Consider the analog signal $x_a(t) = 3 \cos 100\pi t$
   i) Determine the minimum sampling rate required to avoid aliasing.
   ii) Suppose that the signal is sampled at the rate $F_s = 200$ Hz what is the discrete time signal obtained after sampling?
   iii) Suppose that the signal is sampled at the rate $F_s = 75$ Hz what is the discrete time signal obtained after sampling?
   iv) What is the frequency $0 < F < F_s/2$ of a sinusoid that yields samples identical to those obtained in part (iii)

   b) State and prove sampling theorem.

2. a) Determine the stability region for the causal system.

$$H(z) = \frac{1}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

   by computing its poles and restricting them to inside of the circle.

   b) Determine the zero state response of the system

$$y(n) = \frac{1}{2} y(n-1) + 4x(n) + 3x(n-1)$$ to the input

$x(n) = e^{j\omega n} u(n)$. What is the steady state response of the system.

3. a) State and prove the multiplication property of DFTs and circular convolution.
   b) By means of the DFT and IDFT, determine the response of the FIR filter with impulse response.

$$h(n) = \{1, \underset{\uparrow}{2}, 3\}$$

   to the input sequence

$$x(n) = \{1, \underset{\uparrow}{2}, 2, 1\}$$

4. Derive the signal flow graph for the N=16 point, radix4 decimation in frequency FFT algorithm in which input sequence is in normal order and the computations are done in place.

5. a) Discuss the design of FIR filter using Keiser window.
   b) Discuss the effect of finite register length in FIR filter design.

6. Discuss the elliptic approximation method for designing Band stop IIR filter.

7. Illustrate briefly on the following:
   a) Pipelining
   b) Retining
   c) Parallel processing

8. Write short notes on any two of the following:
   a) Park-McClellan's method
   b) Butter worth approximation
   c) Design of programmable DSP's

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