Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

MEVD - 203

M.E./M.Tech., II Semester

Examination, June 2016

VLSI Test and Testability

Time : Three Hours

Maximum Marks : 70

Note : i) Attempt any five questions.
ii) All questions carry equal marks.

1. a) Explain IC production test process and burn-in-board.
   b) Explain different levels of testing. Also discuss design for testability.

2. a) Discuss different types of faults in VLSI circuits during fabrication and packaging.
   b) Describe the transistor faults and delay faults in fault detection process.

3. a) What is simulation? Explain parallel and detective fault simulation.
   b) Briefly explain path sensitization method and its limitation.

4. a) Explain the testing of sequential circuit as iterative combinational circuit.
   b) List various methods for Stuck-at faults. Elaborate any one of them giving suitable example.

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5. a) Describe the testing of sequential circuits as state table verification and random testing.
   b) Discuss the generic offline BIST architecture.

6. a) Explain Ad-Hoc testable design techniques.
   b) Discuss Full scan and Partial scan design.

7. a) Discuss IDDQ testing with importance in VLSI design.
   b) Explain BIST implementation in hardware design.

8. Write short notes on any two
   a) Controllability and observability
   b) CMOS testing
   c) Fault collapsing
   d) Boundary scans

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