

## M. E./M. Tech. (Second Semester) EXAMINATION, Oct., 2009 VLSI TEST AND TESTABILITY

(Elective – I)

[MEVD – 203(A)]

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 40

**Note :** Attempt any *five* questions. All questions carry equal marks. Assume and mention suitable missing data any.

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1. Show that for a fractional increase  $\Delta$  in the area  $A$  of VLSI chip when hardware for design for testability is added the cost increase is given by :

$$\left[ (1 + \Delta) \left( 1 + \frac{A d \Delta}{\alpha + A d} \right)^\alpha - 1 \right] \times 100 \text{ percent}$$

where  $d$  is the defect density and  $\alpha$  is the defect clustering parameter. Calculate the percentage cost increase if the original chip area is  $1 \text{ cm}^2$ ,  $d = 1.25 \text{ defects/cm}^2$ ,  $\alpha = 0.5$  and the area overhead is 10%, i. e.  $\Delta = 0.1$ .

2. Show that for a cluster fault distribution, if the required defect level is  $DL$ , then the fault coverage of tests should be :

$$T = \frac{(\beta + A f)(1 - DL)^{1/\beta} - \beta}{A f} \times 100 \text{ percent}$$

where  $f$  is fault density,  $\beta$  is fault clustering parameter and  $A$  is chip area.

3. Show that the two faults  $C S-a-0$  and  $f S-a-1$  are equivalent in the circuit of fig. 1.

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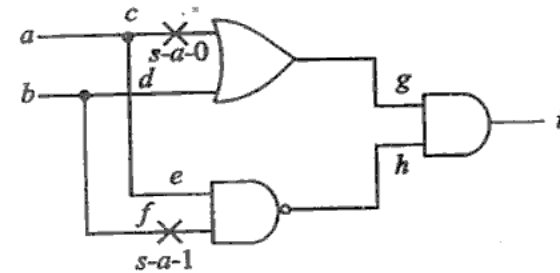


Fig. 1

4. Explain why the reverse-order fault simulation is not a practical test compaction technique for sequential circuits.
5. For a two-input AND gate and a two-input Exclusive-OR gate, develop the singular cover of the gates, the propagation D-Cubes, and primitive D-Cubes of failure for a  $Sa 1$  fault on one of the gate inputs.
6. Use Roth's D-algorithm to perform ATPG for the  $SaO$  fault on the Fan out branch gate  $g$  to  $h$  for the circuit in ahead fig. 2.

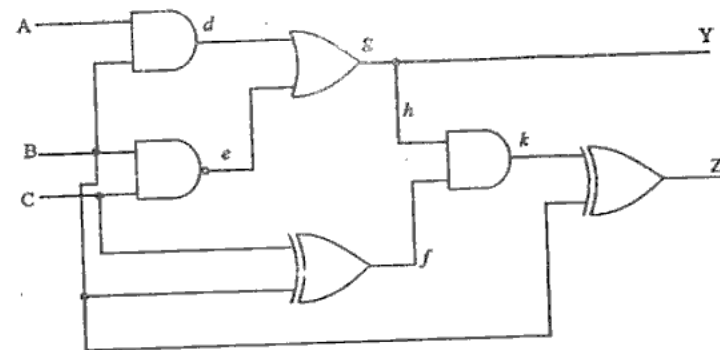


Fig. 2

7. Explain how serial-scan testing is implemented.
8. Explain how a pseudo-random sequence generator (PRSG) may be used to test a 16-bit datapath. How would the outputs be collected and checked ?

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