MTDE - 201 ELECTRONIC SYSTEM DESIGN

UNIT -I  DESIGN CONCEPTS & LOGIC CIRCUITS

Digital Hardware, Design Process, Design of Digital Hardware
Variables & Functions Logic gates & Networks synthesis, SOP, POS forms, Introduction to VHDL.

UNIT- II OPTIMIZED IMPLEMENTATION OF LOGIC FUNCTIONS:

Strategy for minimization, Incompletely specified functions, Multiple output circuits, Multilevel synthesis & Analysis Building Block of combinational circuits, Multiplexers Decoders, Encoders Code Converters.

UNIT- III SYNCHRONOUS SEQUENTIAL CIRCUITS

Basic Design Steps, Mealy state Model, Design of FSM,

UNIT – IV ASYNCHRONOUS SEQUENTIAL CIRCUITS

Analysis, Synthesis, State Reduction, State Assignment, Hazards.

UNIT V  TESTING OF LOGIC CIRCUITS

Fault Model, Path sensitizing, Random testing, Circuits with Tree Structure.

BOOK:
1. Introduction to Logic Design – MARCOVITZ – (Text )

REFERENCES:
1. Engineering Digital Design – TINDER
2. An Engineering Approach to Digital Design – FLETCHER
3. Logic and Computer Design Fundamentals – MANO
UNIT -I

UNIT -II
Digital Filter design: FIR filter design, IIR filter design from analog filters, digital filter design based on least square method.

UNIT -III
Multirate Digital Signal Processing: Decimation & Interpolation, Sampling rate conversion, Filter design and implementation for sampling rate conversion, applications of multirate signal processing

UNIT -IV
Filter Banks: QMF, M-Channel uniform and non-uniform filter banks, transmultiplexers.

UNIT -V
Wavelets: Introduction, the short-time Fourier transform, the wavelet transform, discrete-time orthonormal wavelets, continuous-time orthonormal wavelets.

References
2. P.P.Vaidyanathan, “Multirate Systems and Filter Banks”, Pearson
MTDE – 203 MICROELECTRONIC

1. Introduction to IC Technology, Overview of MOS and BJT, Threshold Voltage, Body effect, basic DC equations, 2nd order Effect, MOS model, small-signal AC characteristics, CMOS inverter and its DC characteristics, static load MOS inverter.

2. Silicon semiconductor technology, wafer processing, oxidation, epitaxy, deposition, ion implantation, CMOS technology, N-Well and P-Well process and SOI.


4. CMOS Logic gate design, Fan-in and Fan-out, typical NAND and NOR delays, Transistor sizing, CMOS logic structure, DC analysis of Complementary Logic, BiCMOS logic, Pseudo NMOS, dynamic CMOS logic, Pass transistor, CMOS Domino Logic, NP domino logic, Cascode voltage switch logic, source-follower pull-up logic (SFPL).

5. Memory cells and Arrays, Clocking disciplines, Design, Power optimization.

6. Fault Modeling and Simulation, Testability, Analysis Technique, Ad-hoc Methods and General guidelines, Scan Technique, Boundary Scan, Built in Self Test, Physics of Interconnects in VLSI, Scaling of Interconnects.

7. PLA Minimization – PLA folding, Fault model in PLA, Test generation and Testable PLA Design.

Text Books:

Reference Books:
MTDE – 204 EMBEDDED SYSTEM

UNIT -I

UNIT -II

UNIT -III
32 bit Micro controller: Intel 80960-architecture, memory address space, Salient features of ARM processor family-ARM7 /ARM9/ ARM9E/ ARM10/ ARM11/ SecureCore /Strong ARM, XScale technology, ARM9200 Architecture, Pinouts, Peripheral Identifier, System Interrupts, External Interrupts, Product memory mapping, External memory mapping, Internal memory mapping, On chip Peripherals-Memory controllers, external Bus Interface(EBI), Advanced interrupt controller(AIC), USART, Timer counter.

UNIT -IV

UNIT -V
Real Time Operating Systems: Task and Task States, tasks and data, semaphores and shared Data Operating system Services- Message queues- Timer Function- Events-Memory Management, Interrupt Routines in an RTOS environment, basic design Using RTOS.

References:
MTDE – 205 FAULT TOLERANT SYSTEMS

UNIT-I

Basic concepts of Reliability: Failures and faults, Reliability and failure rate, Relation between reliability & mean time between failure, Maintainability & Availability, reliability of series and parallel systems. Modeling of faults. Test generation for combinational logic circuits :conventional methods (path sesitisation,Boolean difference), Random testing, transition count testing and signature analysis.

UNIT-II

Fault Tolerant Design-I: Basic concepts ,static,(NMR,use of error correcting codes), dynamic, hybrid and self purging redundancy, Sift-out Modular Redundancy (SMR), triple modular redundancy, SMR reconfiguration.

UNIT-III

Fault Tolerant Design-II: Time redundancy, software redundancy, fail-soft operation, examples of practical fault tolerant systems, introduction to fault tolerant design of VLSI chips.

UNIT-IV

Self checking circuits: Design of totally self checking checkers, checkers using m-out of a codes, Berger codes and low cost residue code, self-checking sequential machines, partially self-checking circuits. Fail safe Design: Strongly fault secure circuits, fail-safe design of sequential circuits using partition theory and Berger codes, totally self checking PLA design.

UNIT-V

Design for testable combination logic circuits: Basic concepts of testability, controllability and observability. The Read-Muller expansion technique, level OR-AND-OR design, use of control and syndrome-testing design.

Built-in-test, built-in-test of VLSI chips, design for autonomous self-test, design in testability into logic boards.

Suggested Reading:
1. Parag K. Lala, Fault Tolerant & Fault Testable Hardware Design,(PHI) 1985