## EC-705 VLSI Design

#### **UNIT I**

# Practical Consideration and Technology in VLSI Design

Introduction, Size and complexity of Integrated Circuits, The Microelectronics Field, IC Production Process, Processing Steps, Packaging and Testing, MOS Processes, NMOS Process, CMOS Process, Bipolar Technology, Hybrid Technology, Design Rules and Process Parameters.

## **UNIT II**

## **Device Modeling**

Dc Models, Small Signal Models, MOS Models, MOSFET Models in High Frequency and small signal, Short channel devices, Sub threshold Operations, Modeling Noise Sources in MOSFET's, Diode Models, Bipolar Models, Passive component Models.

#### **UNIT III**

#### **Circuit Simulation**

Introduction, Circuit Simulation Using Spice, MOSFET Model, Level 1 Large signal model, Level 2 Large Signal Model, High Frequency Model, Noise Model of MOSFET, Large signal Diode Current, High Frequency BJT Model, BJT Noise Model, Temperature Dependence of BJT.

## **UNIT IV**

## **Structured Digital Circuits and Systems**

Random Logic and Structured Logic Forms, Register Storage Circuits, Quasi Static Register Cells, A Static Register Cell, Micro coded Controllers, Microprocessor Design, Systolic Arrays, Bit-Serial Processing Elements, Algotronix.

#### **UNIT V**

## **CMOS Processing Technology**

Basic CMOS Technology, A Basic n-well CMOS Process, Twin Tub Processes, CMOS Process Enhancement, Interconnects and Circuit Elements, Layout Design Rules, Latch up, Physical Origin, Latch up Triggering, Latch up Prevention, Internal Latch up Prevention Techniques.

#### **References:**

- 1. Geiger, Allen and Strader: VLSI Design Techniques for Analog and Digital Circuits, TMH.
- 2. Sorab Gandhi: VLSI Fabrication Principles, Wiley India.
- 3. Weste and Eshraghian: Principles of CMOS VLSI design, Addison-Wesley
- 4. Weste, Harris and Banerjee: CMOS VLSI Design, Pearson-Education.
- 5. Pucknell and Eshraghian: Basic VLSI Design, PHI Learning.
- 6. Sze: VLSI Technology, TMH.