Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

EC-221

B.E., III Semester

Examination, December 2016

Choice Based Credit System (CBCS)

Digital Circuits and System

Time : Three Hours

Maximum Marks : 60

Note: i) Attempt any five questions.
ii) All questions carry equal marks.

1. a) Convert the following:
   i) $(010011110111.1101)_2$ to Hexadecimal
   ii) $(327.4)_8$ to 8's compliment and 7's compliment
   iii) $(231.25)_8$ to Decimal
   b) Draw the k-map for the functions

   $F_\alpha = AB + BD + \overline{A}\overline{B}C$ and $F_\beta = \overline{A}B + B\overline{D}$

   Hence draw k-maps for function $F_1 = F_\alpha F_\beta$ and $F_2 = F_\alpha + F_\beta$. Simplify the maps for F_1 and F_2.

2. a) Minimize Boolean function and implement with only NAND gates

   $F = (\overline{A}B + ACD)(ABC + \overline{A}D + C)$

   b) Prove the following using DeMorgan's theorem:

   $AB + CD = \overline{\overline{AB} \cdot \overline{CD}}$

   Hence prove that an AND-OR configuration is equivalent to NAND-NAND configuration.

3. a) Explain the construction of full subtractor using half subtractor.
   b) Design a 4-bit adder with carry look ahead using logic gates.

4. a) What is master-slave flip-flop? How race around condition is avoided in master-slave flip-flop?
   b) Convert JK flip-flop to SR flip-flop.

5. a) Explain the difference between synchronous and asynchronous counter? Why is synchronous counters faster than asynchronous counter?
   b) Draw the diagram of 4-bit ripple counter and explain with suitable waveform.

6. a) Draw the diagram of TTL NAND gate and explain its working.
   b) Draw and explain the VI characteristics of CMOS inverter.

7. a) Differentiate between different types of ROM.
   b) How combinational circuit can be implemented using PLA.

8. Write short notes on (any three)
   a) Parity generator
   b) T flip-flop
   c) Modulo-n-counter
   d) PAL
   e) SOP and POS minimization techniques

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