Roll No. ....

EC-505

B. E. (Fifth Semester) EXAMINATION, Dec., 2011

(Electronics & Communication Engg. Branch)

CMOS VLSI DESIGN

(EC – 505)

Time : Three Hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt any *one* question from each Unit. All Units are compulsory to attempt. All questions carry equal marks.

Unit – I

1. (a) Explain the CMOS Inverter D. C. characteristic. How CMOS Inverter can be used as amplifier ? 10

   (b) Determine the type and the amount of Channel Ion Implantations which are necessary to achieve a threshold voltage of $VT_0 = -2\,V$ for P-Channel mosfet with the following parameters : 10

   (i) Substrate doping density $N_A = 10^{15}/cm^3$

   (ii) Polysilicon gate doping density $N_D = 10^{20}/cm^3$

   (iii) $T_{OX} = 650\,\text{Å}$

   (iv) $N_{OX} = 4 \times 10^{10}/cm^2$

   Also calculate threshold voltage V_{T_0} for $V_{SB} = 0$.

Or

2. (a) Write short notes on the following :   12
   (i)   Stick diagrams
   (ii) Channel length modulation
   (iii) Pass transistor
   (iv) Tunneling

   (b) Explain briefly the MOS capacitance model.   8

Unit – II

3. (a) Explain the following terms in reference of VLSI technology :   20
   (i)   Wafer formation
   (ii) Photolithography
   (iii) Oxidation
   (iv) Isolation
   (v)   Well and Channel formation

Or

4. (a) What are VLSI interconnects ? How interconnects are developed during IC fabrication ?   10

   (b) What are design rules ? Explain MOSIS Design rule.   10

Unit – III

5. (a) Explain Elmore's delay model for estimation of parasitic delay in CMOS circuit.   10

   (b) Explain the following terms with respect to CMOS chip design :   10
   (i)   Capacitance
   (ii) Process variation
   (iii) Temperature
   (iv) Reliability

Or

6. (a) What is power dissipation in CMOS ? Explain static power dissipation and its cause. Explain different methods to reduce it. 12

   (b) Explain the following terms : 8
   (i) Transmission sizing
   (ii) Interconnect scaling

Unit – IV

7. (a) What are CMOS Op-Amp. and RF circuits ? Explain them briefly. 10

   (b) What are differential pains ? Explain them in brief with mathematical expression ? 10

Or

8. (a) What are current mirrors ? Derive expression for it. 10

   (b) Explain the following : 10
   (i) MOS Small Signal Model
   (ii) CMOS designed Analog to Digital Converter

Unit – V

9. Explain the following terms : 20
   (i) Cell Hierarchies
   (ii) Cell Shapes
   (iii) Ratioed circuit
   (iv) Cascode Voltage Switch logic

Or

10. What is BICMOS logic ? Derive the expression for switching delay in BICMOS logic circuit ? Explain different applications of BICMOS. 20

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