Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

EC-701-CBGS

B.Tech., VII Semester

Examination, December 2020

Choice Based Grading System (CBGS)

VLSI Design

Time : Three Hours

Maximum Marks : 70

Note: i) Attempt any five questions.

ii) All questions carry equal marks.

1. a) Summarize the equation for describing the channel length modulation effect in NMOS transistor.

   b) Draw the DC transfer characteristics of CMOS inverter.

2. a) Design a symbolic layout for a complementary CMOS circuit that implements F= A + BC

   b) Explain the architecture for low power VLSI design.

3. a) Derive the propagation delay PHLτ for inverter.

   b) What are the different simulations available to test a combinational circuits? Explain them.

4. a) Design a full adder by cascading two half adders and develop a project to realize it in model simulator 6.0.

   b) List out all the methods of design strategies for test and explain any three methods

5. a) Draw and explain the Data path test scheme for chip level test methods.

   b) Draw the physical layout for the following Boolean expression.

      i) y = (a +b)' + c + de

      ii) x = (lmnop)' + q'(r's + rs')

6. a) Briefly explain VLSI IC circuits design flow with figure.

   b) Write brief notes on:

      i) Twin-Tube process

      ii) Silicon - On Insulator (SOI) process.

7. a) What is wires and vias? How to design them.

   b) What are different layout design rules? Explain them with suitable examples.

8. a) Write brief notes on:

      i) Algotronics

      ii) Latchup Triggering

   b) Comment on the procedure/process of Microprocessor Design.

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