Roll No ..

EE - 504
B.E. V Semester
Examination, December 2015
Digital Electronics and Logic Design

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.

ii) All parts of each questions are to be attempted at one place.

iii) All questions carry equal marks, out of which part A and B (Max.50 words) carry 2 marks, part C (Max.100 words) carry 3 marks, part D (Max.400 words) carry 7 marks.

iv) Except numericals, Derivation, Design and Drawing etc.

Unit-I

1. a) Convert $(11010111.110)_2$ to decimal and hexadecimal numbers.

b) Subtract $(3250 – 72532)_{10}$ using 10's complement.

c) Express the number $(8620)_{10}$ in BCD and excess 3-code.

d) Explain error detecting and correcting codes with examples.

OR

Explain weighted and non-weighted codes with example.

Unit-II

2. a) Implement EX-OR using NAND gates only.

b) Implement the given function using NAND gates
$F(A, B, C) = \Sigma m(0, 6)$.

c) Implement the function using universal gates only
$f = xy + x\bar{y}$.

d) Draw a TTL circuit with totem pole output and explain its working. Why should it not be used for wired AND connection?

OR

Write short notes on : ECL Logic Family.

Unit-III

3. a) Explain encoders with diagram.

b) Explain multiplexers with diagram.

c) Express the Boolean function $F = \overline{AC + BC}$ in a sum of minterms.

d) Minimize the following Boolean expression using K-map and realize it using the basic gates.

$f = \Sigma m(1, 3, 5, 9, 11, 13)$

OR

A combinational circuit is defined by the functions :

$F_1 (A, B, C) = \Sigma (3, 5, 6, 7)$

$F_2 (A, B, C) = \Sigma (0, 2, 47)$

Implement the circuit with a PLA having 3-inputs, 4-product terms and two-outputs.

Contd...

Unit-IV

4. a) Obtain excitation table of JK-Flip-Flop.

   b) Convert T-Flip-Flop to D-Flip-Flop.

   c) For a toggle flip-flop, write the state table, draw the state diagram and write the state equations.

   d) Explain the designing features and working of a 3-bit bidirectional shift-register with parallel load.

OR

By using suitable ffs, design a counter to go through the states 0-1-3-4-6-0. Draw the logic diagram. Examine the active of counter for the unused states.

Unit-V

5. a) Calculate the number of address and data lines of 256K × 4 IC.

   b) Compare RAM and ROM.

   c) Explain the concept of memory decoding.

   d) Explain ROM and its working. How is it different from PLA.

OR

Explain the dual-slope converter.

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