Total No. of Questions :5] *[Total No. of Printed Pages :2*

Roll No .....

EX - 304 (New)

B.E. III Semester

Examination, December 2015

Electronic Devices

Time : Three Hours

Maximum Marks : 70

Note: i) Answer five questions. In each question part A, B, C is compulsory and D part has internal choice.
ii) All parts of each question are to be attempted at one place.
iii) All questions carry equal marks, out of which part A and B (Max. 50 words) carry 2 marks, part C (Max. 100 words) carry 3 marks, part D (Max. 400 words) carry 7 marks.
iv) Except numericals, Derivation, Design and Drawing etc.

1. a) What are energy band diagram? Explain with references to p-type and n-type semiconductors.
   b) What is potential barrier? Explain with reference to p-n junction diode.
   c) Discuss Hall effect in brief.
   d) Draw and explain VI characteristic of a p-n junction diode. Also give expressions for various current components.

   OR

   Find the factor by which the reverse saturation current of Ge and Si diodes increases when the temperature changes from 27°C to 77°C.

2. a) Give specific characteristics of zener diode.
   b) What are the characteristics of a varactor diode? Explain in brief.
   c) Give working principle of a Schottky-diode.
   d) Elaborate the working of clipper and clamper circuits with the help of neat diagrams.

   OR

   Draw circuit diagram of a bridge rectifier and explain its working with its merit and demerits. Also draw all input and output waveforms.

3. a) What is Early effect? Explain in brief.
   b) What are the regions of operation of BJT? Explain.
   c) Define α and β of a BJT.
   d) Draw CC, CB and CE configurations for BJT and compare these for their characteristic parameters.

   OR

   Determine various current components and region of operation for the BJT-circuit shown ahead in Figure 1.

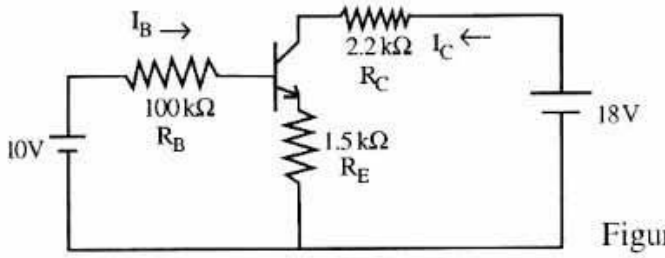

Figure 1

4. a) Give h-parameters for CE-configuration.
   b) Explain one technique far bias compensation using diode in brief.
   c) What are the various steps involved in drawing the DC-load line and locating the Q-point.
   d) Draw circuit for voltage divider (Self-bias) bias technique and derive expression for stability factor.

   OR

   Design the voltage divider bias circuit to have $V_{CE} = 15V$ $I_C = 15mA$ given that $V_{CC} = 30V$, $V_{BE} = 0.7V$, $R_C = 2k\Omega$ $h_{FE} = 50$ and stability factor $S \leq 5$.

5. a) Enlist general properties of FET.
   b) What are the differences between n-channel and p-channel FET's?
   c) Discuss features of Depletion-type MOSFET.
   d) Give one technique of biasing of n-channel JFET with its merits and demerits.

   OR

   Draw circuit diagram of CD amplifier (source follower) and give its equivalent circuit. Find expression for its voltage gain.

******