

EXPERIMENT NO...1

AIM:

To verify the Demorgan's theorems.

APPARATUS REQUIRED:

Digital logic trainer and Patch cords.

THEORY:

The digital signals are discrete in nature and can only assume one of the two values 0 and 1. A number system based on these two digits is known as binary number system. This is basic of all digital systems like computers, calculators etc.

Binary Variables can be represented by letter symbol such A,B,X,Y.

The variable can have only one of the two variable possible values at anytime i.e. '0' or '1' Demorgan's Theorems can be proved by first considering the two variable case and then extending this result.

DEMORGAN'S THEOREM'S:

$$\overline{A+B+C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$$
$$\overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$$

PROCEDURE:

DEMORGAN'S THE -1

$$\overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$$

1. Make the circuit dia. As in fig and connect the inputs of the gate to the input state sockets A,B and C and output to the output indicators.
2. Set the input combinations one by one by putting input state switches A,B and C either in 0 or 1 state.
3. Now verify the output with the help of Truth Table (1)

TRUTH TABLE (1)

A	B	C	A	B	C	A.B.C	A.B.C	A+B+C
0	0	0	1	1	1	0	1	1
0	0	1	1	1	0	0	1	1
0	1	0	1	0	1	0	1	1
0	1	1	1	0	0	0	1	1
1	0	0	0	1	1	0	1	1
1	0	1	0	1	0	0	1	1
1	1	0	0	0	1	0	1	1
1	1	1	0	0	0	1	0	0

DEMORGAN'S THEOREM-2:

$$\overline{A+B+C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

Make the circuit dia. As shown in fig and connect the inputs of the gate to the input state sockets A,B and C and output to the output indicators.

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1. Set the input combinations one by the putting input state switches A,B and C either '0' or '1' state.
2. Now verify the output with the help of Truth Table (2).

TRUTH TABLE (2)

A	B	C	A	B	C	A.B.C	A+B+C	A+B+C
0	0	0	1	1	1	0	1	1
0	0	1	1	1	0	1	0	0
0	1	0	1	0	1	1	0	0
0	1	1	1	0	0	1	0	0
1	0	0	0	1	1	1	0	0
1	0	1	0	1	0	1	0	0
1	1	0	0	0	1	1	0	0
1	1	1	0	0	0	1	0	0

RESULT:

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Experiment No.2

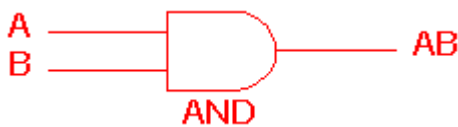
Aim: To study and verify the Truth Tables of AND, OR, NOT, NAND, NOR EXOR logic gates for positive logic.

Apparatus Required:

Digital logic trainer and Patch cords

Theory:

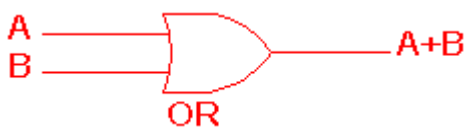
AND Gate: A multi-input circuit in which the output is 1 only if all inputs are 1. The symbolic representation of the AND gate is:



2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

The AND gate is an electronic circuit that gives a high output (1) only if all its inputs are high. A dot (.) is used to show the AND operation i.e. A.B .

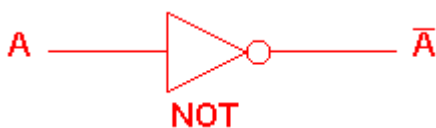
OR gate : A multi-input circuit in which the output is 1 when any input is 1. The symbolic representation of the OR gate is shown:



2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

The OR gate is an electronic circuit that gives a high output (1) if one or more of its inputs are high. A plus (+) is used to show the OR operation.

NOT gate: The output is 0 when the input is 1, and the output is 1 when the input is 0. The symbolic representation of an inverter is :



NOT gate	
A	\bar{A}
0	1
1	0

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an inverter. If the input variable is A, the inverted output is known as NOT A. This is also shown as A', or A with a bar over the top, as shown at the outputs.

NAND gate: AND followed by INVERT. It is also known as universal gate. The symbolic representation of the NAND gate is:

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2 Input NAND gate		
A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if any of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

NOR gate: OR followed by inverter. It is also known as universal gate. The symbolic representation is:



2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if any of the inputs are high. The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

EXOR gate: The output of the Exclusive –OR gate, is 0 when it's two inputs are the same and it's output is 1 when its two inputs are different. It is also known as Anti-coincidence gate.



2 Input EXOR gate		
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

The 'Exclusive-OR' gate is a circuit which will give a high output if either, but not both, of its two inputs are high. An encircled plus sign (\oplus) is used to show the EOR operation.

Observation Table: LED ON(RED light): Logic 1
 LED OFF(Green Light): Logic 0
 Input variables: A ,B
 Output variable: Y

S.No	Input(A) LED	Input(B) LED	Output (OR) — $Y = A + B$	Output (AND) — $Y = AB$	Output (OR) — $Y = A + B$	Output (NAND) — $Y = \overline{AB}$	Output (NOR) — $Y = \overline{A+B}$	Output (XOR) — $Y = A \oplus B$
1								
2								
3								
4								

Calculation:

Results and Analysis:

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NOT Gate: When logic 1 is applied to one of NOT gate of 7404 IC, then output becomes zero. When input LED is ON (RED), the output LED become OFF (Green) vice versa.

OR Gate: The output of an OR gate is a 1 if one or the other or both of the inputs are 1, but a 0 if both inputs are 0. When One or the other or Both of the input LEDS are ON (RED Light), then output LED is ON(RED) otherwise Output LED is OFF(Green Light)

AND Gate: The output of an AND gate is only 1 if both its inputs are 1. For all other possible inputs the output is 0. When both the LEDS are On, then output LED is ON (RED Light) otherwise Output LED is OFF.

NOR Gate: The output of the NOR gate is a 1 if both inputs are 0 but a 0 if one or the other or both the inputs are 1.

NAND Gate: The output of the NAND gate is a 0 if both inputs are 1 but a 1 if one or the other or both the inputs are 0.

EXOR gate: The output of the XOR gate is a 1 if either but not both inputs are 1 and a 0 if the inputs are both 0 or both 1.

RESULT:

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EXPERIMENT NO...3

AIM: - To verify the Half Adder & Full Adder

APPARATUS REQUIRED:

Digital logic trainer and Patch cords.

THEORY:

Half Adder

With the help of half adder, we can design circuits that are capable of performing simple addition with the help of logic gates.

Let us first take a look at the addition of single bits.

$$0+0 = 0$$

$$0+1 = 1$$

$$1+0 = 1$$

$$1+1 = 10$$

These are the least possible single-bit combinations. But the result for 1+1 is 10. Though this problem can be solved with the help of an EXOR Gate, if you do care about the output, the sum result must be re-written as a 2-bit output.

Thus the above equations can be written as

$$0+0 = 00$$

$$0+1 = 01$$

$$1+0 = 01$$

$$1+1 = 10$$

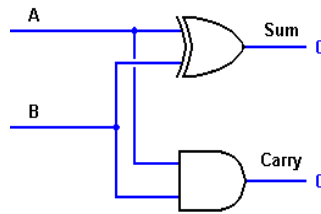
Here the output '1' of '10' becomes the carry-out. The result is shown in a truth-table below. 'SUM' is the normal output and 'CARRY' is the carry-out.

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

From the equation it is clear that this 1-bit adder can be easily implemented with the help of EXOR Gate for the output 'SUM' and an AND Gate for the carry. Take a look at the implementation below.

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For complex addition, there may be cases when you have to add two 8-bit bytes together. This can be done only with the help of full-adder logic.

Full Adder

This type of adder is a little more difficult to implement than a half-adder. The main difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry designated as CIN. When a full adder logic is designed we will be able to string eight of them together to create a byte-wide adder and cascade the carry bit from one adder to the next.

The output carry is designated as COUT and the normal output is designated as S. Take a look at the truth-table.

INPUTS		OUTPUTS		
A	B	CIN	COUT	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

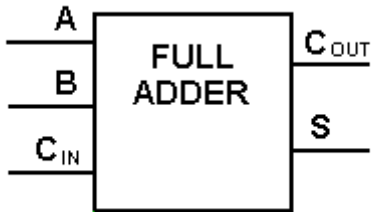
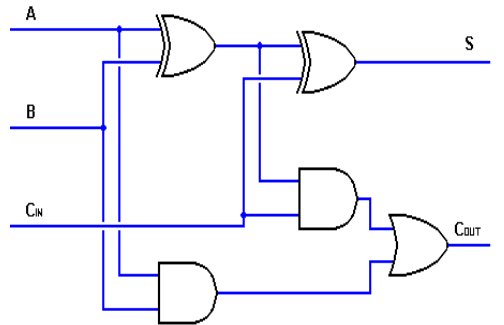
From the above truth-table, the full adder logic can be implemented. We can see that the output S is an EXOR between the input A and the half-adder SUM output with B and CIN inputs. We must also note that the COUT will only be true if any of the two inputs out of the three are HIGH.

Thus, we can implement a full adder circuit with the help of two half adder circuits. The first half adder will be used to add A and B to produce a partial Sum. The second half adder logic can be used to

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add C_{IN} to the Sum produced by the first half adder to get the final S output. If any of the half adder logic produces a carry, there will be an output carry. Thus, C_{OUT} will be an OR function of the half-adder Carry outputs.



Single Bit full Adder

With this type of symbol, we can add two bits together taking a carry from the next lower order of magnitude, and sending a carry to the next higher order of magnitude. In a computer, for a multi-bit operation, each bit must be represented by a full adder and must be added simultaneously. Thus, to add two 8-bit numbers, you will need 8 full adders which can be formed by cascading two of the 4-bit blocks. The addition of two 4-bit numbers is shown below.

RESULT:

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EXPERIMENT NO...4

AIM:

To verify the Hlf Substactor & Full Substractor

APPARATUS REQUIRED:

Digital logic trainer and Patch cords.

THEORY

The arithmetic operation, subtraction of two binary digits has four possible elementary operations, namely,

$$0 - 0 = 0$$

$$0 - 1 = 1 \text{ with 1 borrow}$$

$$1 - 0 = 1$$

$$1 - 1 = 0$$

In all operations, each subtrahend bit is subtracted from the minuend bit. In case of the second operation the minuend bit is smaller than the subtrahend bit, hence 1 is borrowed.

HALF SUBTRACTOR:

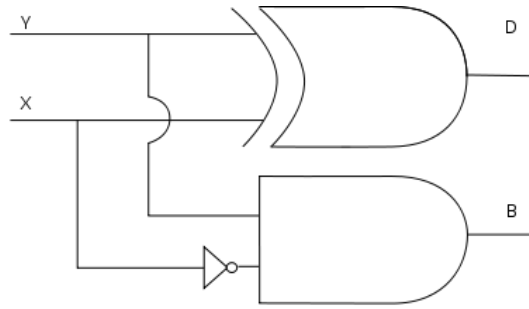
A combinational circuit which performs the subtraction of two bits is called half subtractor. The input variables designate the minuend and the subtrahend bit, whereas the output variables produce the difference and borrow bits. **Half subtractor**

The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow).

INPUTS		OUTPUTS	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

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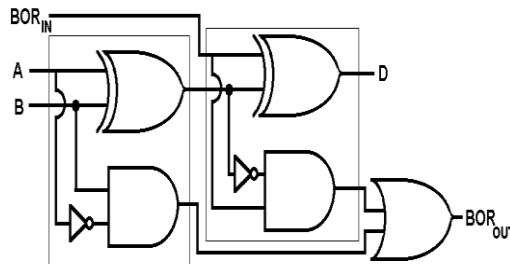
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Full subtractor

A combinational circuit which performs the subtraction of three input bits is called full subtractor. The three input bits include two significant bits and a previous borrow bit. A full subtractor circuit can be implemented with two half subtractors and one OR gate. As in the case of the addition using logic gates, a full subtractor is made by combining two half-subtractors and an additional OR-gate. A full subtractor has the borrow in capability (denoted as BOR_{IN} in the diagram below) and so allows cascading which results in the possibility of multi-bit subtraction. The circuit diagram for a full subtractor is given below.

INPUTS		OUTPUTS		
A	B	CIN	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



RESULT:

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EXPERIMENT NO...5

AIM: -To verify the characteristic table of RS, D, JK, and T Flip flops .

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	NOR gate	IC 7402	
3.	NOT gate	IC 7404	
4.	AND gate (three input)	IC 7411	
5.	NAND gate	IC 7400	
6.	Connecting wires		As required

THEORY:

A Flip Flop is a sequential device that samples its input signals and changes its output states only at times determined by clocking signal. Flip Flops may vary in the number of inputs they possess and the manner in which the inputs affect the binary states.

RS FLIP FLOP:

The clocked RS flip flop consists of NAND gates and the output changes its state with respect to the input on application of clock pulse. When the clock pulse is high the S and R inputs reach the second level NAND gates in their complementary form. The Flip Flop is reset when the R input high and S input is low. The Flip Flop is set when the S input is high and R input is low. When both the inputs are high the output is in an indeterminate state.

D FLIP FLOP:

To eliminate the undesirable condition of indeterminate state in the SR Flip Flop when both inputs are high at the same time, in the D Flip Flop the inputs are never made equal at the same time. This is obtained by making the two inputs complement of each other.

JK FLIP FLOP:

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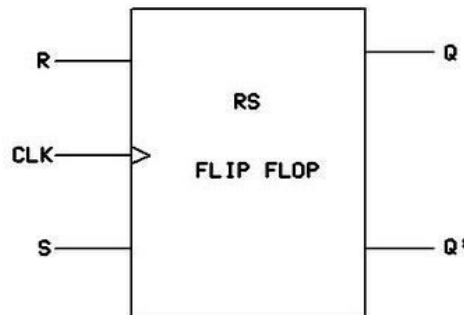
The indeterminate state in the SR Flip-Flop is defined in the JK Flip Flop. JK inputs behave like S and R inputs to set and reset the Flip Flop. The output Q is ANDed with K input and the clock pulse, similarly the output Q' is ANDed with J input and the Clock pulse. When the clock pulse is zero both the AND gates are disabled and the Q and Q' output retain their previous values. When the clock pulse is high, the J and K inputs reach the NOR gates. When both the inputs are high the output toggles continuously. This is called Race around condition and this must be avoided.

T FLIP FLOP:

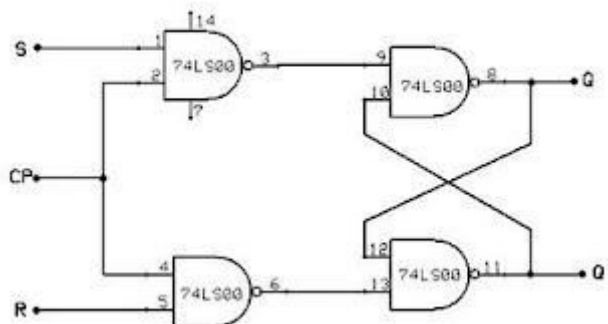
This is a modification of JK Flip Flop, obtained by connecting both inputs J and K inputs together. T Flip Flop is also called Toggle Flip Flop.

RS FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:



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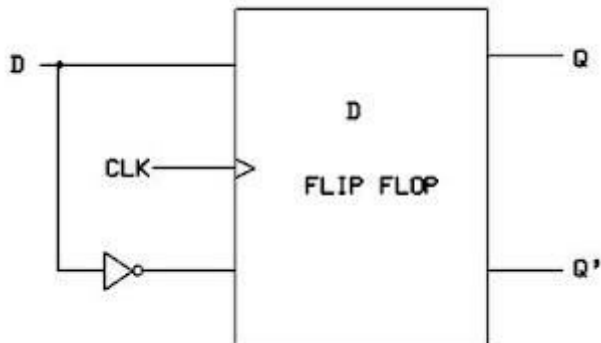
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CHARACTERISTIC TABLE:

CLOCK PULSE	INPUT		PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
	S	R			
1	0	0	0	0	
2	0	0	1	1	
3	0	1	0	0	
4	0	1	1	0	
5	1	0	0	1	
6	1	0	1	1	
7	1	1	0	X	
8	1	1	1	X	

D FLIP FLOP

LOGIC SYMBOL:



CHARACTERISTIC TABLE:

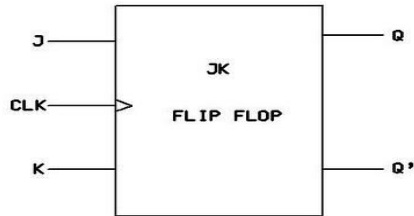
CLOCK PULSE	INPUT D	PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
1	0	0	0	
2	0	1	0	
3	1	0	1	
4	1	1	1	

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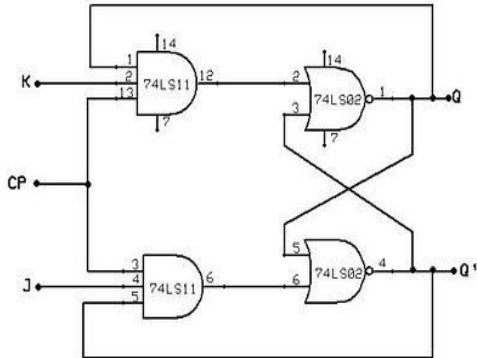
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JK FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:



CHARACTERISTIC TABLE:

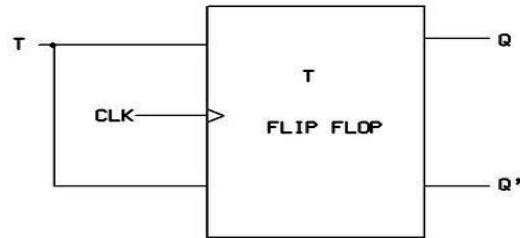
CLOCK PULSE	INPUT		PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
	J	K			
1	0	0	0	0	
2	0	0	1	1	
3	0	1	0	0	
4	0	1	1	0	
5	1	0	0	1	
6	1	0	1	1	
7	1	1	0	1	
8	1	1	1	0	

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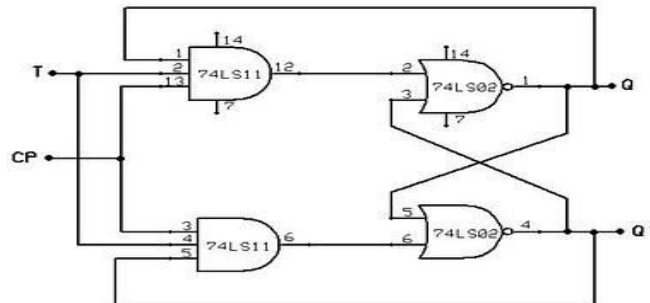
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T FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:



CHARACTERISTIC TABLE:

CLOCK PULSE	INPUT T	PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
1	0	0	0	
2	0	1	0	
3	1	0	1	
4	1	1	0	

PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
3. Apply the inputs and observe the status of all the flip flops.

RESULT:

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Experiment No. 06

AIM:

The main objective of this experiment is to study the working principle of 4:1 multiplexer.

APPARATUS REQUIRED:

Trainer Kit, 230V power supply.

THEORY:

S multiplexers are circuits that can select one of many inputs. 4:1 is the most popular multiplexer and as the name indicates it has 4 inputs with only 1 output. It has 2 data selector inputs namely S_0, S_1 , at which the control bits are applied.

S_0, S_1 are the point at which the controls are applied. D_0, D_1 , represent the inputs bits. Only one of these will be transmitted to the output. But which one of the inputs will be transmitted will depend on the values of the controls. If for instance $S_1 S_0=00$, then the first AND gate is enabled and all others are disabled. Hence D_0 is transmitted. Again if $S_2 S_1=01$, then the second AND enable and D_1 will be transmitted. It is the control nibble that decide which inputs will be transmitted. Therefore, an input D_n is selected corresponding to the decimal number 'n' representing $S_1 S_0$.

PROCEDURE:

1. Connect 2 pin power cord of the trainer to the 230V supply.
2. Make strobe switch at low position.
3. Set the data inputs (D_0-D_{15}) to either 0 or 1.
4. To verify the multiplexer action set the address line as shown in the truth table & observe the output condition.
5. Observe the effect of strobe input on the output.

TRUTH TABLE

s_1	s_0	y
0	0	x_0
0	1	x_1
1	0	x_2
1	1	x_3

RESULT:

The truth table of the mux is verified from the theoretical truth table.

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EXPERIMENT No:07

AIM:

Study of working principle of 1:4 demultiplexer using IC-44145

APPARATUS REQUIRED:

Trainer kit, power supply.

THEORY:

Demultiplexer as the name indicates, it has only data input D with 4 outputs namely Y₀, Y₁, Y₂, Y₃. It has two data selector inputs namely S₀, S₁, at which control bits are applied.

The data bit is transmitted to the data bit Y₀, Y₁, Y₂, Y₃ of the output lines. Which particular output line will be chosen will depend on the value of S₁, S₀ the control input. Consider the case when S₁ S₀=00 now the upper AND gate is enable while all other AND gate are disabled. Hence it is not possible to activate any output other than Y₀. Thus Y₀=D, if D is low Y₀ will be low and if D is high, Y₀ will be high. Considering another case, S₁, S₀=01. We find that Y₁ is activated because second AND gate is enable. Similarly if S₁ S₀=11. The sixteenth AND gate will be enabled and Y₁₅ Will be activated. Thus if D is high then all values other then the correct value of activated Y output, will be low.

PROCEDURE:

1. Connect 2 pin power cord of trainer to 230V supply.
2. Make strobe switch at low position.
3. Set the data input (D₀-D₁₅) to either 0 or 1
4. To verify the Demultiplexer action, set the address line as shown n in truth table and observe the output condition.
5. Observe the effect of strobe input on the output.

RESULT:

The truth Table for 1:4 Demultiplexer is verified.

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Data Input	Select Inputs		Outputs			
D	S_1	S_0	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

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EXPERIMENT NO...8

AIM:

To study the Encoder and Decoder Circuits.

APPARATUS REQUIRED:

Encoder and Decoder kit, patch cords etc.

THEORY:

Combinational logic circuit are digital circuits made up to gates and inverters. An example of this type is the Exclusive OR circuit. The most common type are Decoders, Multiplexers, Comparators and Convertors.

A widely used type of decoder is the BCD To decimal Decoder, the input to the decoder is a parallel 4-Bit Binary number from 0000 through 1001 and the circuit provides ten discrete outputs representing decimal numbers 0 through 9. The output of such a decoder is generally used to operate a lighted number display. Some codes are 8-4-2-1 binary code (Natural BCD), Excess-3 code and gray code. 4 bits are required to represent the decimal digits in these codes.

An Encoder is a combinational logic circuit that essentially performs a “reverse” decoder function. An encoder accepts and active one of its inputs representing a digit, such as a decimal digit or octal digit and converts it to a coded output, such as a binary or BCD. Encoders can also be devised to encode various symbols and alphabetic characters. This process of converting from familiar symbols or numbers to a coded format is called ‘Encoding’.

PROCEDURE:

A. Decimal to BCD Encoder:

1. Connect nine logic inputs of IC 74147 to logic inputs ‘0’ & ‘1’ through patch cords.
2. Connect four logic outputs to outputs indicators through patch cords.
3. Switch ON the instrument using ON/OFF toggle switch provided on the front panel
4. Verify the observation Table no (1). X means either “0” or “1”.

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OBSERVATION TABLE (1)

Decimal Inputs									BCD Outputs			
1	2	3	4	5	6	7	8	9	Q _D	Q _C	Q _B	Q _A
1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0
X	0	1	1	1	1	1	1	1	1	1	0	1
X	X	0	1	1	1	1	1	1	1	1	0	0
X	X	X	0	1	1	1	1	1	1	0	1	1
X	X	X	X	0	1	1	1	1	1	0	1	0
X	X	X	X	X	0	1	1	1	1	0	0	1
X	X	X	X	X	X	0	1	1	1	0	0	0
X	X	X	X	X	X	X	0	1	0	1	1	1
X	X	X	X	X	X	X	9	0	0	1	1	0

B. Binary to Gray Code Converter:1

1. Connect four logic inputs (A,B,C,D) OF Binary to gray code convertor to logic inputs 0 & 1 through path cords.
2. Connect four logic outputs (Q_A,Q_B,Q_C&Q_D) of the convertor to four logic output indicators through patch cords.
3. Switch ON the instrument using ON/OFF toggle switch provided on front panel.
4. Verify the observation table (2)

D	C	B	A	Q _D	Q _C	Q _B	Q _A
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1

C. BCD to Decimal Decoder:

1. Connect four logic inputs (A,B,C,D) of BCD to Decimal code convertor to logic inputs 0 & 1 through patch cords.
2. Connect ten logic outputs of the convertor to ten logic output indicators through patch cords.
3. Switch ON the instrument using ON/OFF toggle switch provided front panel.
4. Verify the observation table (3).

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OBSERVATION TABLE (3)

BCD Inputs				Decimal Outputs									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	0	1	1	1	0	1	1	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	1	1	1	1	1	1	1	1	0	1	1	1
0	1	1	0	1	1	1	1	1	1	1	0	1	1
1	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	0	1	1	1	1	1	1	1	1	1	0

D. BCD to 7- segment Decoder:

1. Connect four logic inputs (A,B,C,D) OF BCD to 7- Segment Decoder to logic inputs 0 & 1 through patch cords.
2. Connect seven logic outputs (Q₁ ,Q₂,Q₃,Q₄,Q₅,Q₆,Q₇) of the convertor to inputs of 7-segment display through patch cords i.e. connect Q₁ output to resistance R₁,Q₂ to R₂,Q₃ to R₃,Q₄, to R₄ and so on..
3. Switch ON the instrument using ON/OFF toggle switch provided on front panel.
4. Verify the observation table (4).

OBSERVATION TABLE (4)

BCD Inputs				7-Segment
D	C	B	A	Outputs
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

RESULT:

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EXPERIMENT No:09

AIM: -To design and verify the truth table of a 4X1 Multiplexer & 1X4 Demultiplexer.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	OR gate	IC 7432	
3.	NOT gate	IC 7404	
4.	AND gate (three input)	IC 7411	
5.	Connecting wires		As required

THEORY:

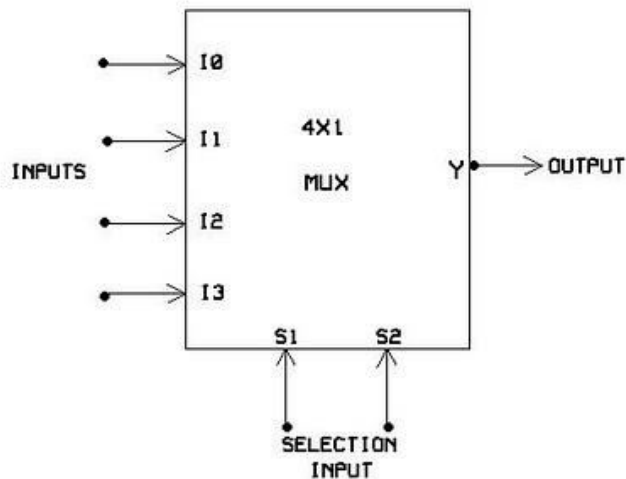
Multiplexer is a digital switch which allows digital information from several sources to be routed onto a single output line. The basic multiplexer has several data input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selector lines whose bit combinations determine which input is selected. Therefore, multiplexer is 'many into one' and it provides the digital equivalent of an analog selector switch.

A Demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of specific output line is controlled by the values of n selection lines.

DESIGN:

4 X 1 MULTIPLEXER

LOGIC SYMBOL:



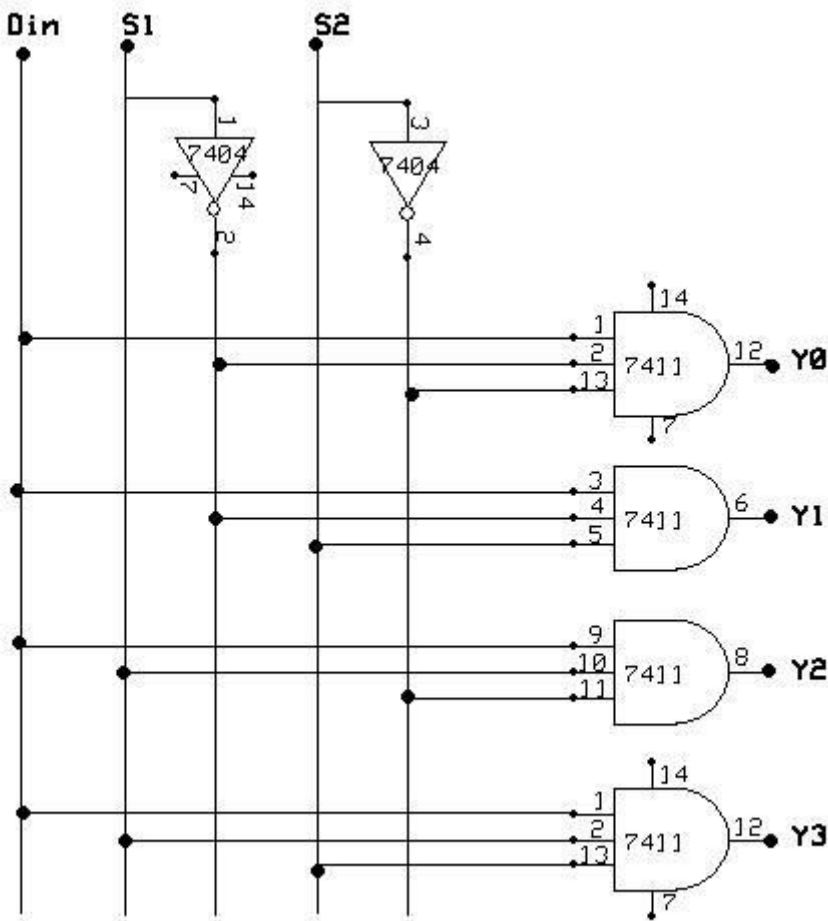
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TRUTH TABLE:

S.No	SELECTION INPUT		OUTPUT
	S1	S2	Y
1.	0	0	I_0
2.	0	1	I_1
3.	1	0	I_2
4.	1	1	I_3

CIRCUIT DIAGRAM:

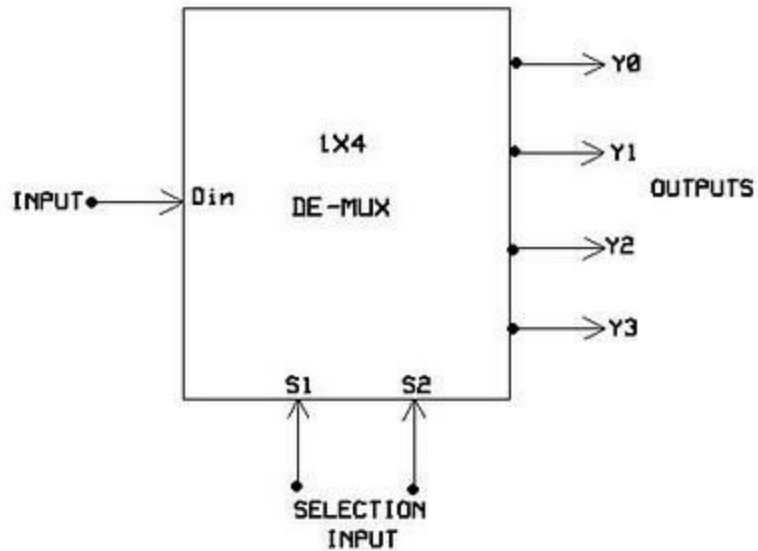


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1X4 DEMULTIPLEXER

LOGIC SYMBOL:



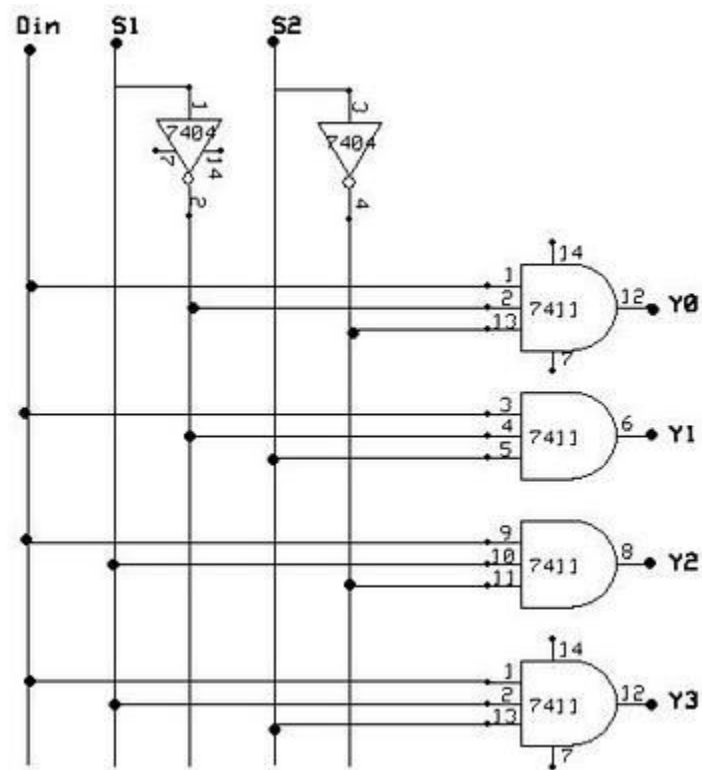
TRUTH TABLE:

S.No	INPUT			OUTPUT			
	S1	S2	Din	Y0	Y1	Y2	Y3
1.	0	0	0	0	0	0	0
2.	0	0	1	1	0	0	0
3.	0	1	0	0	0	0	0
4.	0	1	1	0	1	0	0
5.	1	0	0	0	0	0	0
6.	1	0	1	0	0	1	0
7.	1	1	0	0	0	0	0
8.	1	1	1	0	0	0	1

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CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the multiplexer & demultiplexer.

RESULT: