College Name, BHOPAL

Laboratory Manual

For

EDC

Submitted to:

Submitted By:

College Name , City

Department of Electronics and Communication.

Electronic Devices and Circuit

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Electronic Devices and Circuit

Experiment no. 1

Title: To observe front panel control knobs and to find amplitude, time period and frequency for given waveforms.

APPARATUS: CRO Function generator and probes

PROCEDURE

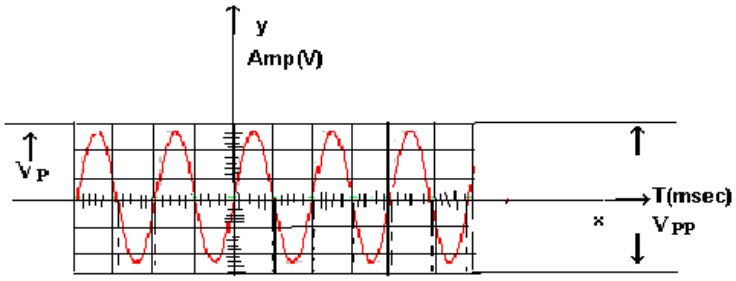
1. Understand the significance of each and every knob on the CRO.
2. From the given function generator feed in a sinusoidal wave and adjust the time base knob and the amplitude knob to observe the waveforms a function of time.
3. Measure the time period and amplitude (peak to peak) of the signal. Find the frequency and verify if the same frequency is given from the function generator.
4. Observe two waveforms simultaneously on the two channels of a CRO.
5. Repeat the above steps for pulse and triangular waveforms.
6. Report the readings and the waveforms taken.

MEASUREMENTS:

Amplitude = no. of vertical divisions * Volts/div.

Time period = no. of horizontal divisions * Time/div. Frequency=(1/T)Hz

MODELGRAPHS:



APPLICATIONS OF CRO:

1. Measurement of current
2. Measurement of voltage
3. Measurement of power
4. Measurement of frequency
5. Measurement of phase angle
6. To see transistor curves
7. To trace and measuring signals of RF, IF and AFin radio and TV.
8. To trace visual display of sine waves.

Do and Don'ts to be strictly observed during experiment:

Do (*<u>also go through the General Instructions</u>*):

1. Before making the connection, identify the components leads, terminal or pins before making the connections.
2. Before connecting the power supply to the circuit, measure voltage by voltmeter/multimeter.
3. Use sufficiently long connecting wires, rather than joining two or three small ones.
4. The circuit should be *switched off* before changing any connection.

Don'ts:

1. Avoid loose connections and short circuits on the bread board.
2. Do not exceed the voltage while taking the readings.
3. Any live terminal shouldn't be touched while supply is on.

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Experiment no. 2

Title: V-I characteristics of p-n-Junction Diode

Objectives:

- To understand the basic concepts of semiconductors.
- To study p type and n type semiconductor and potential barrier.
- To understand forward and reverse biasing.
- Perform the experiment on bread board and the trainer kit and plot the graph of V-I characteristics of PN junction diode.

Components and equipments required: single strand cable, diode, resistors, bread board, multimeter, connecting wires, CRO, voltage source.

General Instructions: You will plan for Experiment after self study of Theory given below, before entering in the Lab.

Theory:

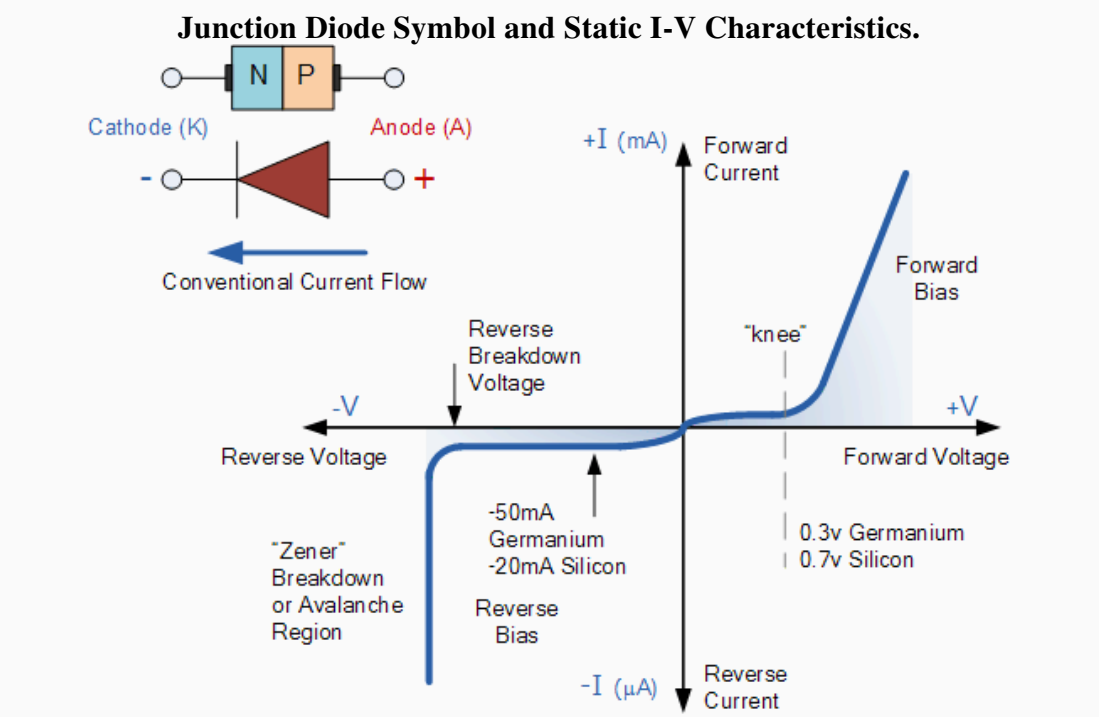
PN Junction Diode

The effect described in the previous tutorial is achieved without any external voltage being applied to the actual PN junction resulting in the junction being in a state of equilibrium. However, if we were to make electrical connections at the ends of both the N-type and the P-type materials and then connect them to a battery source, an additional energy source now exists to overcome the barrier resulting in free charges being able to cross the depletion region from one side to the other. The behavior of the PN junction with regards to the potential barrier width produces an asymmetrical conducting two terminal device, better known as the **Junction Diode**.

A diode is one of the simplest semiconductor devices, which has the characteristic of passing current in one direction only. However, unlike a resistor, a diode does not behave linearly with respect to the applied voltage as the diode has an exponential I-V relationship and therefore we cannot described its operation by simply using an equation such as Ohm's law.

If a suitable positive voltage (forward bias) is applied between the two ends of the PN junction, it can supply free electrons and holes with the extra energy they require to cross the junction as the width of the depletion layer around the PN junction is decreased. By applying a negative voltage (reverse bias) results in the free charges being pulled away from the junction resulting in the depletion layer width being increased. This has the effect of increasing or decreasing the effective resistance of the junction itself allowing or blocking current flow through the diode.

Then the depletion layer widens with an increase in the application of a reverse voltage and narrows with an increase in the application of a forward voltage. This is due to the differences in the electrical properties on the two sides of the PN junction resulting in physical changes taking place. One of the results produces rectification as seen in the PN junction diodes static I-V (current-voltage) characteristics. Rectification is shown by an asymmetrical current flow when the polarity of bias voltage is altered as shown below.



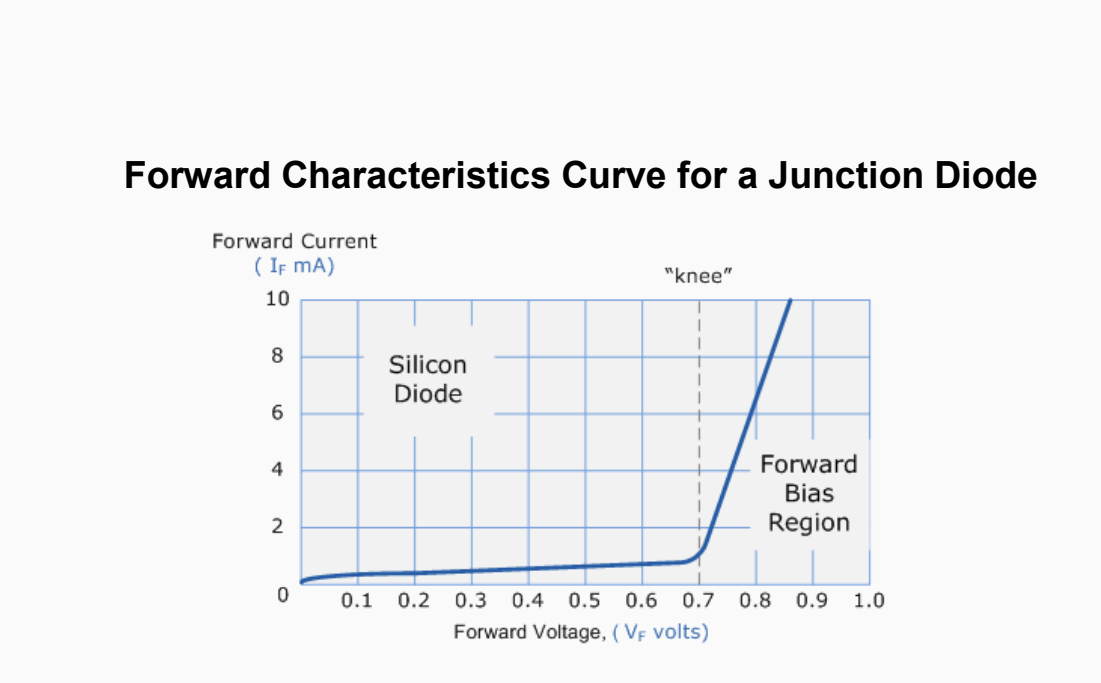
But before we can use the PN junction as a practical device or as a rectifying device we need to firstly **bias** the junction, ie connect a voltage potential across it. On the voltage axis above, "Reverse Bias" refers to an external voltage potential which increases the potential barrier. An external voltage which decreases the potential barrier is said to act in the "Forward Bias" direction.

There are two operating regions and three possible "biasing" conditions for the standard **Junction Diode** and these are:

1. Reverse Bias - The voltage potential is connected negative, (-ve) to the P-type material and positive, (+ve) to the N-type material across the diode which has the effect of **Increasing** the PN-junction width.
2. Forward Bias - The voltage potential is connected positive, (+ve) to the P-type material and negative, (-ve) to the N-type material across the diode which has the effect of **Decreasing** the PN-junction width.

Forward Biased Junction Diode

When a diode is connected in a Forward Bias condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow. This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage. This results in a characteristics curve of zero current flowing up to this voltage point, called the "knee" on the static curves and then a high current flow through the diode with little increase in the external voltage as shown below.



The application of a forward biasing voltage on the junction diode results in the depletion layer becoming very thin and narrow which represents a low impedance path through the junction thereby allowing high currents to flow. The point at which this sudden increase in current takes place is represented on the static I-V characteristics curve above as the "knee" point.

This condition represents the low resistance path through the PN junction allowing very large currents to flow through the diode with only a small increase in bias voltage. The actual potential difference across the junction or diode is kept constant by the action of the depletion layer at approximately 0.3v for germanium and approximately 0.7v for silicon junction diodes. Since the diode can conduct "infinite" current above this knee point as it effectively becomes a short circuit, therefore resistors are used in series with the diode to limit its current flow. Exceeding its maximum forward current specification causes the device to dissipate more power in the form of heat than it was designed for resulting in a very quick failure of the device.

Reverse Biased Junction Diode

- When a diode is connected in a Reverse Bias condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material. The positive voltage applied to the N-type material attracts electrons towards the positive

electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode. The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

Procedure:

Forward bias:

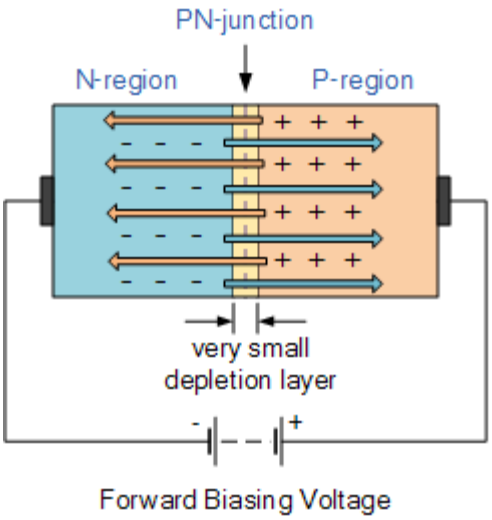
1. Make the connections as shown in fig.:
2. Switch on the power supply.
3. Now vary in small step the forward bias voltage and current readings on multimeter. Draw the graph between current and voltage.

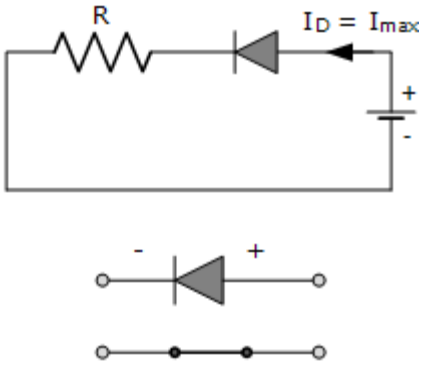
Reverse bias:

1. Make the connection as shown in fig:
2. Switch on the power supply.

Observation:

Forward biasing

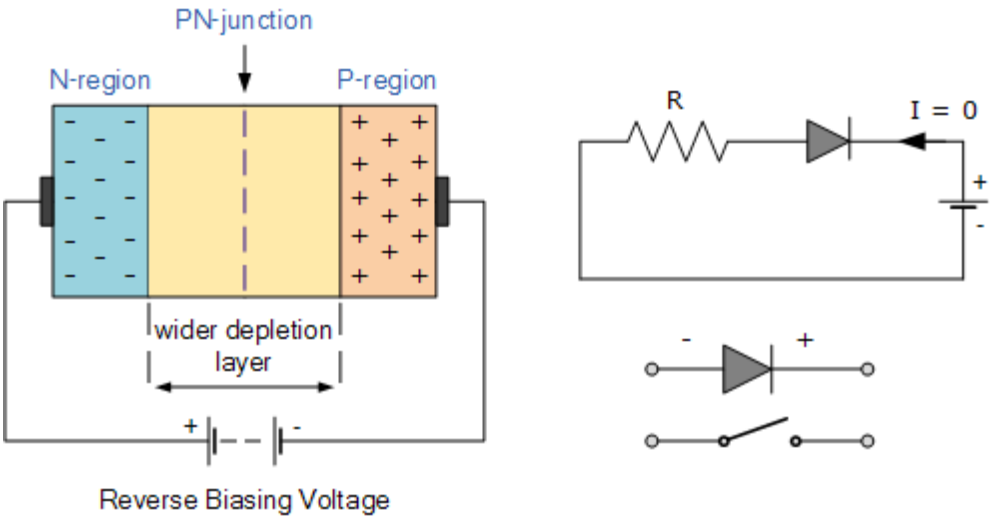




Observation Table:

Sr. no	V_F	I_F *(mA)*

Reverse biasing:



Observation Table:

Sr. no	V_R	I_R *(μA)*

Do and Don'ts to be strictly observed during experiment:

Do (*<u>also go through the General Instructions</u>*):

1. Before making the connection, identify the components leads, terminal or

pins before making the connections.

2. Before connecting the power supply to the circuit, measure voltage by voltmeter/multimeter.
3. Use sufficiently long connecting wires, rather than joining two or three small

ones.

4. The circuit should be *switched off* before changing any connection.

Don’ts:

1. Avoid loose connections and short circuits on the bread board.
2. Do not exceed the voltage while taking the readings.
3. Any live terminal shouldn't be touched while supply is on.

Outputs: Submit the graph as per observation table.

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Electronic Devices and Circuit [EC – 303]

Experiment no. 3

Title: To Study half wave and full wave rectifier.

Objectives:

- To understand the basic concept of diodes and rectifiers.
- To study the types of rectifiers.
- Perform the experiment on the trainer kit
- Observe the waveforms of half wave and full wave rectifier.
- Find percentage of regulation.

Components and equipments required: Rectifiers trainer, CRO, multimeter, set of patching wires.

General Instructions: You will plan for Experiment after self study of Theory given below, before entering in the Lab.

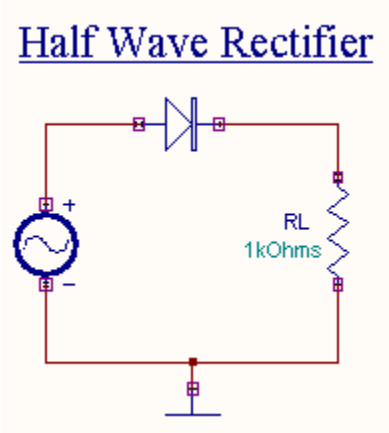
Theory:

RECTIFIER

A rectifier is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which flows in only one direction. The process is known as rectification. Physically, rectifiers take a number of forms, including vacuum tube diodes, mercury-arc valves, solid-state diodes, silicon-controlled rectifiers and other silicon-based semiconductor switches.

HALFWAVE RECTIFIER

The Half wave rectifier is a circuit, which converts an ac voltage to dc voltage. In the Half wave rectifier circuit shown above the transformer serves two purposes. It can be used to obtain the desired level of dc voltage (using step up or step down transformers). It provides isolation from the power line. The primary of the transformer is connected to ac supply. This induces an ac voltage across the secondary of the transformer. During the positive half cycle of the input voltage the polarity of the voltage across the secondary forward biases the diode. As a result a current IL flows through the load resistor, RL. The forward biased diode offers a very low resistance and hence the voltage drop across it is very small. Thus the voltage appearing across the load is practically the same as the input voltage at every instant.



During the negative half cycle of the input voltage the polarity of the secondary voltage gets reversed. As a result, the diode is reverse biased. Practically no current flows through the circuit and almost no voltage is developed across the resistor. All input voltage appears across the diode itself. Hence we conclude that when the input voltage is going through its positive half cycle, output voltage is almost the same as the input voltage and during the negative half cycle no voltage is available across the load. This explains the unidirectional pulsating dc waveform obtained as output. The process of removing one half the input signal to establish a dc level is aptly called half wave rectification.

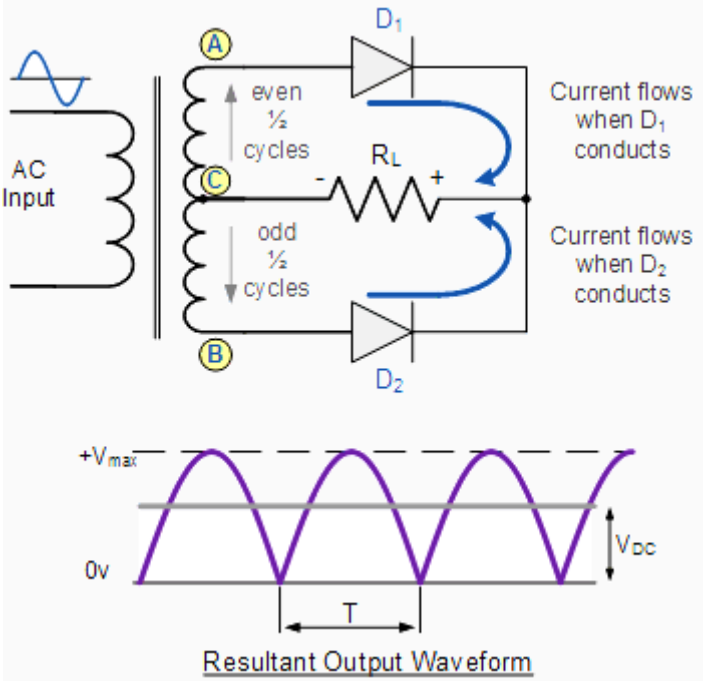
The Full Wave Rectifier

In the previous **Power Diodes** tutorial we discussed ways of reducing the ripple or voltage variations on a direct DC voltage by connecting capacitors across the load resistance. While this method may be suitable for low power applications it is unsuitable to applications which need a "steady and smooth" DC supply voltage. One method to improve on this is to use every half-cycle of the input voltage instead of every other half-cycle. The circuit which allows us to do this is called a **Full Wave Rectifier**.

Like the half wave circuit, a full wave rectifier circuit produces an output voltage or current which is purely DC or has some specified DC component. Full wave rectifiers have some fundamental advantages over their half wave rectifier counterparts. The average (DC) output voltage is higher than for half wave, the output of the full wave rectifier has much less ripple than that of the half wave rectifier producing a smoother output waveform.

In a Full Wave Rectifier circuit two diodes are now used, one for each half of the cycle. A transformer is used whose secondary winding is split equally into two halves with a common centre tapped connection, (C). This configuration results in each diode conducting in turn when its anode terminal is positive with respect to the transformer centre point C producing an output during both half-cycles, twice that for the half wave rectifier so it is 100% efficient as shown below.

Full Wave Rectifier Circuit



The full wave rectifier circuit consists of two power diodes connected to a single load resistance (RL) with each diode taking it in turn to supply current to the load. When point A of the transformer is positive with respect to point C, diode D1 conducts in the forward direction as indicated by the arrows. When point B is positive (in the negative half of the cycle) with respect to point C, diode D2 conducts in the forward direction and the current flowing through resistor R is in the same direction for both half-cycles. As the output voltage across the resistor R is the phasor sum of the two waveforms combined, this type of full wave rectifier circuit is also known as a "bi-phase" circuit.

As the spaces between each half-wave developed by each diode is now being filled in by the other diode the average DC output voltage across the load resistor is now double that of the single half-wave rectifier circuit and is about 0.637Vmax of the peak voltage, assuming no losses.

Where: VMAX is the maximum peak value in one half of the secondary winding and VRMS is the rms value.

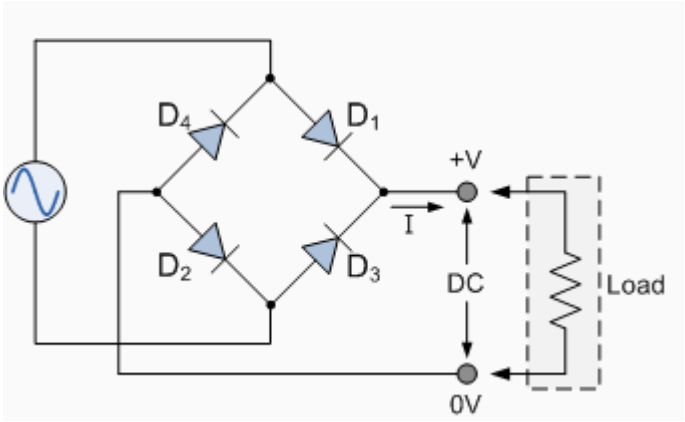
The peak voltage of the output waveform is the same as before for the half-wave rectifier provided each half of the transformer windings have the same rms voltage value. To obtain a different DC voltage output different transformer ratios can be used. The main disadvantage of this type of full wave rectifier circuit is that a larger transformer for a given power output is required with two separate but identical secondary windings making this type of full wave

rectifying circuit costly compared to the "Full Wave Bridge Rectifier" circuit equivalent.

The Full Wave Bridge Rectifier

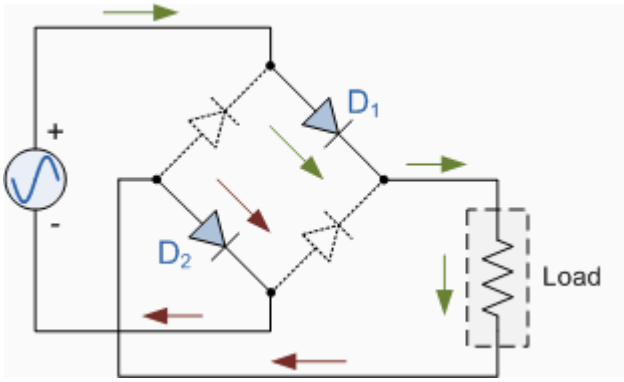
Another type of circuit that produces the same output waveform as the full wave rectifier circuit above, is that of the Full Wave Bridge Rectifier. This type of single phase rectifier uses four individual rectifying diodes connected in a closed loop "bridge" configuration to produce the desired output. The main advantage of this bridge circuit is that it does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown below.

The Diode Bridge Rectifier



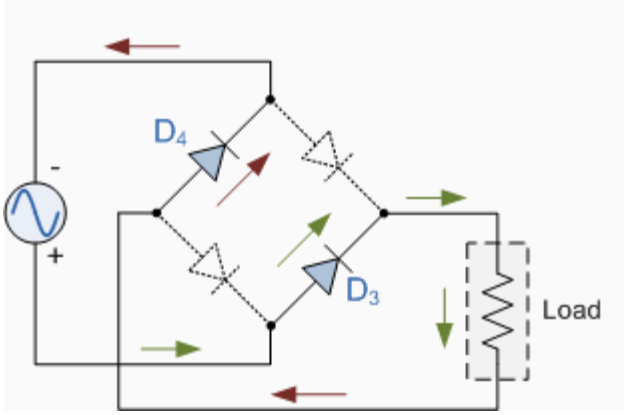
The four diodes labeled D1 to D4 are arranged in "series pairs" with only two diodes conducting current during each half cycle. During the positive half cycle of the supply, diodes D1 and D2 conduct in series while diodes D3 and D4 are reverse biased and the current flows through the load as shown below.

The Positive Half-cycle



During the negative half cycle of the supply, diodes D3 and D4 conduct in series, but diodes D1 and D2 switch "OFF" as they are now reverse biased. The current flowing through the load is the same direction as before.

The Negative Half-cycle



As the current flowing through the load is unidirectional, so the voltage developed across the load is also unidirectional the same as for the previous two diode full-wave rectifier, therefore the average DC voltage across the load is 0.637Vmax. However in reality, during each half cycle the current flows through two diodes instead of just one so the amplitude of the output voltage is two voltage drops (2 x 0.7 = 1.4V) less than the input VMAX amplitude. The ripple frequency is now twice the supply frequency (e.g. 100Hz for a 50Hz supply)

Typical Bridge Rectifier

Although we can use four individual power diodes to make a full wave bridge rectifier, pre-made bridge rectifier components are available "off-the-shelf" in a range of different voltage and current sizes that can be soldered directly into a PCB circuit board or be connected by

spade connectors. The image to the right shows a typical single phase bridge rectifier with one corner cut off. This cut-off corner indicates that the terminal nearest to the corner is the positive or +ve output terminal or lead with the opposite (diagonal) lead being the negative or -ve output lead. The other two connecting leads are for the input alternating voltage from a transformer secondary winding.

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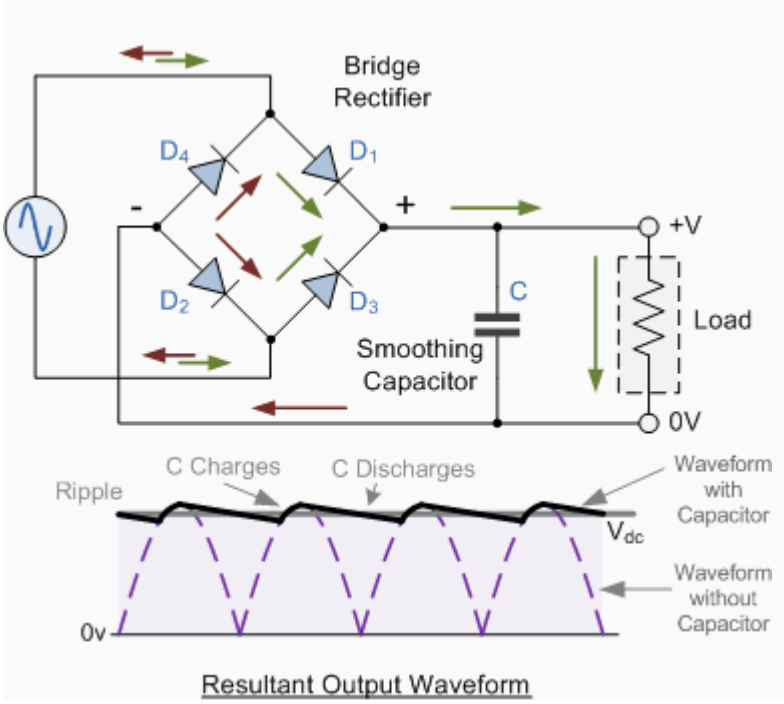

Resultant Output Waveform

Procedure:

1. Make the connections as shown in figure.
2. Give input ac supply.
3. Observe output waveform across load.

Do and Don'ts to be strictly observed during experiment:

Do (*also go through the General Instructions*):

1. Before making the connection, identify the components leads, terminal or pins before making the connections.
2. Before connecting the power supply to the circuit, measure voltage by voltmeter/multimeter.

3. Use sufficiently long connecting wires, rather than joining two or three small ones.
4. The circuit should be *switched off* before changing any connection.

Don’ts:

1. Avoid loose connections and short circuits on the bread board.
2. Do not exceed the voltage while taking the readings.
3. Any live terminal shouldn't be touched while supply is on.

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Electronic Devices and Circuit [EC – 303]

Experiment no. 4

Title: V-I characteristics of Zener Diode.

Objectives:

- To study p type and n type semiconductor.
- To understand reverse biasing.
- To understand breakdown voltage.
- Perform the experiment on the trainer kit and plot the graph of V-I characteristics of Zener diode.

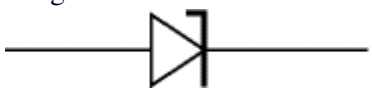
Components and equipments required: Zener diode, multimeter, connecting wires.,power supply.

General Instructions: You will plan for Experiment after self study of Theory given below, before entering in the Lab.

Theory:

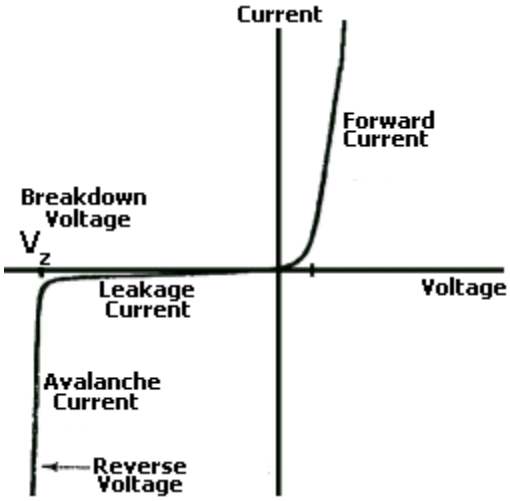
Zener diode

A zener diode is a special kind of diode which allows current to flow in the forward direction in the same manner as an ideal diode, but will also permit it to flow in the reverse direction when the voltage is above a certain value known as the breakdown voltage, "zener knee voltage" or "zener voltage." The device was named after Clarence Zener, who discovered this electrical property. Many diodes described as "zener" diodes rely instead on avalanche breakdown as the mechanism. Both types are used. Common applications include providing a reference voltage for voltage regulators, or to protect other semiconductor devices from momentary voltage pulses. A **Zener Diode** is a special kind of diode which permits current to flow in the forward direction as normal, but will also allow it to flow in the reverse direction when the voltage is above a certain value - the breakdown voltage known as the Zener voltage.



The Zener voltage of a standard diode is high, but if a reverse current above that value is allowed to pass through it, the diode is permanently damaged. Zener diodes are designed so that their zener voltage is much lower - for example just 2.4 Volts. When a reverse current above the Zener voltage

passes through a Zener diode, there is a controlled breakdown which does not damage the diode. The voltage drop across the Zener diode is equal to the Zener voltage of that diode no matter how high the reverse bias voltage is above the Zener voltage.



The illustration above shows this phenomenon in a Current vs. Voltage graph. With a zener diode connected in the forward direction, it behaves exactly the same as a standard diode - i.e. a small voltage drop of 0.3 to 0.7V with current flowing through pretty much unrestricted. In the reverse direction however there is a very small leakage current between 0V and the Zener voltage - i.e. just a tiny amount of current is able to flow. Then, when the voltage reaches the breakdown voltage (Vz), suddenly current can flow freely through it.

Uses of Zener Diodes

Since the voltage dropped across a Zener Diode is a known and fixed value, Zener diodes are typically used to regulate the voltage in electric circuits. Using a resistor to ensure that the current passing through the Zener diode is at least 5mA (0.005 Amps), the circuit designer knows that the voltage drop across the diode is exactly equal to the Zener voltage of the diode.

Procedure:

1. Do the connections of trainer kit.
2. After increasing the battery of Vb to 1v.
3. Measure the current and voltage across Zener diode.
4. Repeat the step 2 and 3 for voltage 2v-10v with the increase in steps of 1v.

Observation table:

Sr. no	***Vb***	$I_z (\mu A)$	V_z

Do and Don’ts to be strictly observed during experiment:

Do (*<u>also go through the General Instructions</u>*):

1. Before making the connection, identify the components leads, terminal or pins before making the connections.
2. Before connecting the power supply to the circuit, measure voltage by voltmeter/multimeter.
3. Use sufficiently long connecting wires, rather than joining two or three small

ones.

4. The circuit should be *switched off* before changing any connection.

Don’ts:

1. Avoid loose connections and short circuits on the bread board.
2. Do not exceed the voltage while taking the readings.
3. Any live terminal shouldn't be touched while supply is on.

Conclusion:

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Experiment no. 5

Title: Input and output characteristics of transistor in common emitter configuration.

Objectives:

- To understand the basic concepts of transistor.
- To study types of transistor.
- To study working of common base transistor in active, saturation and cutoff region.
- Perform the experiment on the trainer kit and plot the input and output characteristics for different values.

Components and equipments required: trainer kit, multimeter and connecting wires.

General Instructions: You will plan for Experiment after self study of Theory given below, before entering in the Lab.

Theory:

A transistor consist of two PN junctions formed by sandwiching P-type or N-type semi-conductor between a pair of opposite type .

According there are two pairs of transistor namely:

1. n-p-n transistor
2. p-n-p transistor

A transistor has three terminals

(i) Emitter (ii) Base (iii) Collector

The emitter is heavily doped so that it can input a large number of change carriers into base. The base is lightly doped and varies thin passes that most of the emitter injected charge carriers to the collector .The collector is moderately doped .The junction between emitter and base called emitter-base junction. The junction between the collector and base may be called as collector –base junction. The emitter junction is always forward biased and collector junction is always reversed biased. A transistor transfer a low resistance circuit to high resistance circuit and hence the name

Trans → transfer, istor → resistance.

Common Emitter Configuration

In this circuit arrangement, input is applied between base and emitter and output is taken out from collector and emitter. Thus emitter is common terminal for input and output signals. Therefore, such circuitry is known as common emitter –configuration.

Procedure:

1. Connect the circuit as shown in this circuit diagram.
2. For input characteristic

(i) Keeping VCE constant (say 1V) ,note down the base current IB for various of VBE.

(ii) Then plot the reading obtained on a graph taking IB along Y-axis and VBE along X-axis.

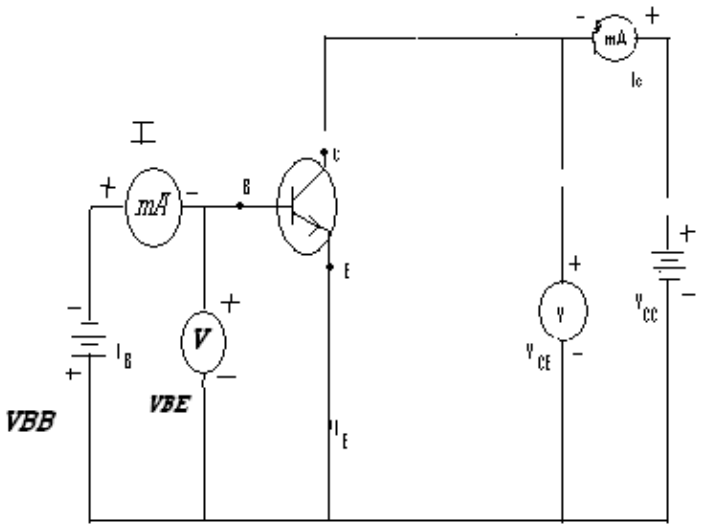
(iii) Repeat the procedures of VCE = 4V or Above 4V.

3. For output characteristic

(i) Keeping IB current constant say(1 microampere) , note down the collector current IC for various values of VCE .

(ii) Plot the reading on a graph taking IC along Y-axis & VCE along X-axis.

(iii)Repeat the procedure for various values of IB.



NPN TRANSISTER IN (CE) MODE

Observation table:

Input characteristics:

S.NO.	VCE = 1V		VCE = 4V		VCE = 6V	
	VBE	IB	VBE	IB	VBE	IB

OUTPUT CHARACTERISTICS

S.NO.	IB = 10μF		IB = 20μF		IB = 30μF	
	VCE (V)	IC (μA)	VCE (V)	IC (μA)	VCE (V)	IC (μA)

Outputs: Submit the graph as per observation table.

Conclusion:

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Experiment no. 6

Title: To study characteristics of FET transistor

Objectives:

- To understand the basic concepts of FET transistor.
- To study types of FET transistor.
- To study working of FET transistor.
- Perform the experiment on the trainer kit and plot the gate and drain characteristics for different values.

Components and equipments required: D.C power supply .Oscilloscope ,multimeter FET, Resistors

General Instructions: You will plan for Experiment after self study of Theory given below, before entering in the Lab.

Theory:

The acronym 'FET' stands for field effect transistor. It is a three-terminal unipolar solidstate device in which current is controlled by an electric field as is done in vacuum tubes.

Broadly speaking, there are two types of FETs :

(a) junction field effect transistor (JFET)

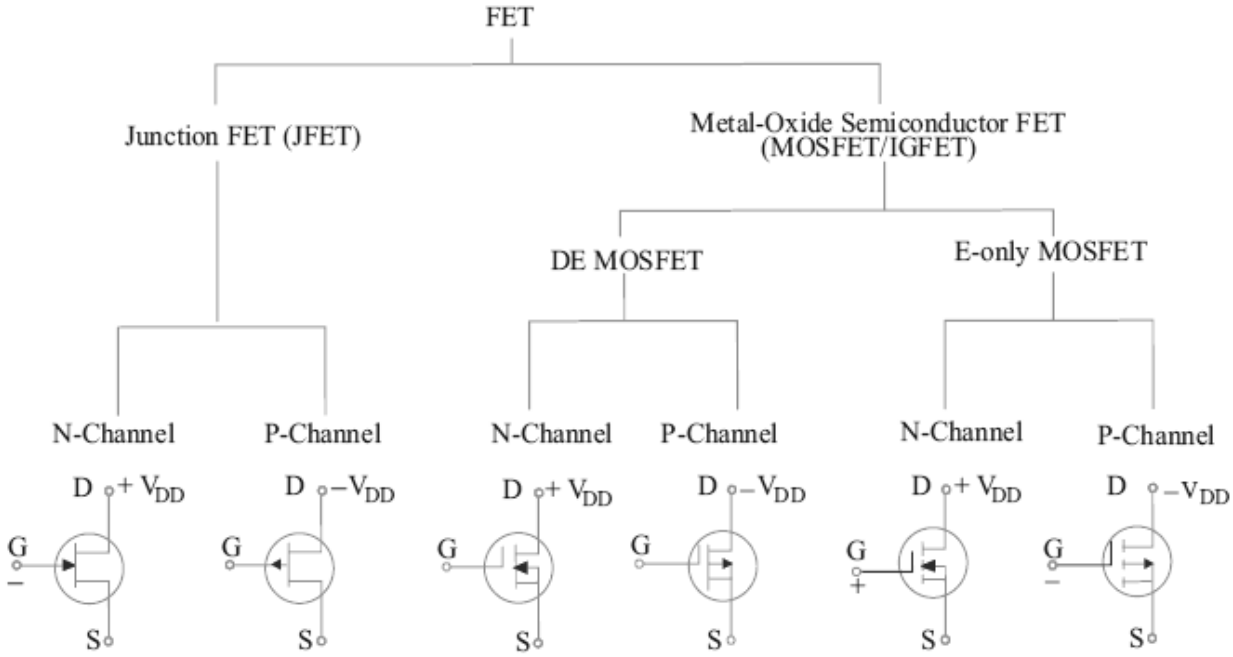
(b) metal-oxide semiconductor FET (MOSFET)

It is also called insulated-gate FET (IGFET). It may be further subdivided into :

(i) depletion-enhancement MOSFET i.e. DEMOSFET

(ii) enhancement-only MOSFET i.e. E-only MOSFET

Both of these can be either P-channel or N-channel devices.



As shown in Fig. it can be fabricated with either an N-channel or P-channel though Nchannel is generally preferred. For fabricating an N-channel JFET, first a narrow bar of Ntype semiconductor material is taken and then two P-type junctions are diffused on opposite sides of its middle part [Fig.1 (a)]. These junctions form two P-N diodes or gates and the areabetween these gates is called channel. The two P-regions are internally connected and a single lead is brought out which is called gate terminal. Ohmic contacts (direct electrical connections) are made at the two ends of the bar-one lead is called source terminal S and the other drain terminal D. When potential difference is established between drain and source, current flows along the length of the 'bar' through the channel located between the two Pregions.

The current consists of only majority carriers which, in the present case, are electrons. P-channel JFET is similar in construction except that it uses P-type bar and two Ntype junctions. The majority carriers are holes which flow through the channel located between the two N-regions or gates.

Following FET notation is worth remembering:

1. Source. It is the terminal through which majority carriers enter the bar. Since carriers come

from it, it is called the source.

2. Drain. It is the terminal through which majority carriers leave the bar i.e. they are drained out from this terminal. The drain to source voltage VDS drives the drain current ID.

3. Gate. These are two internally-connected heavily-doped impurity regions which form two P-N junctions. The gate-source voltage VGS reverse biases the gates.

4. Channel. It is the space between two gates through which majority carriers pass from source-to-drain when VDS is applied.

Schematic symbols for N-channel and P-channel JFET are shown in Fig.1 (c). It must be kept in mind that gate arrow always points to N-type material.

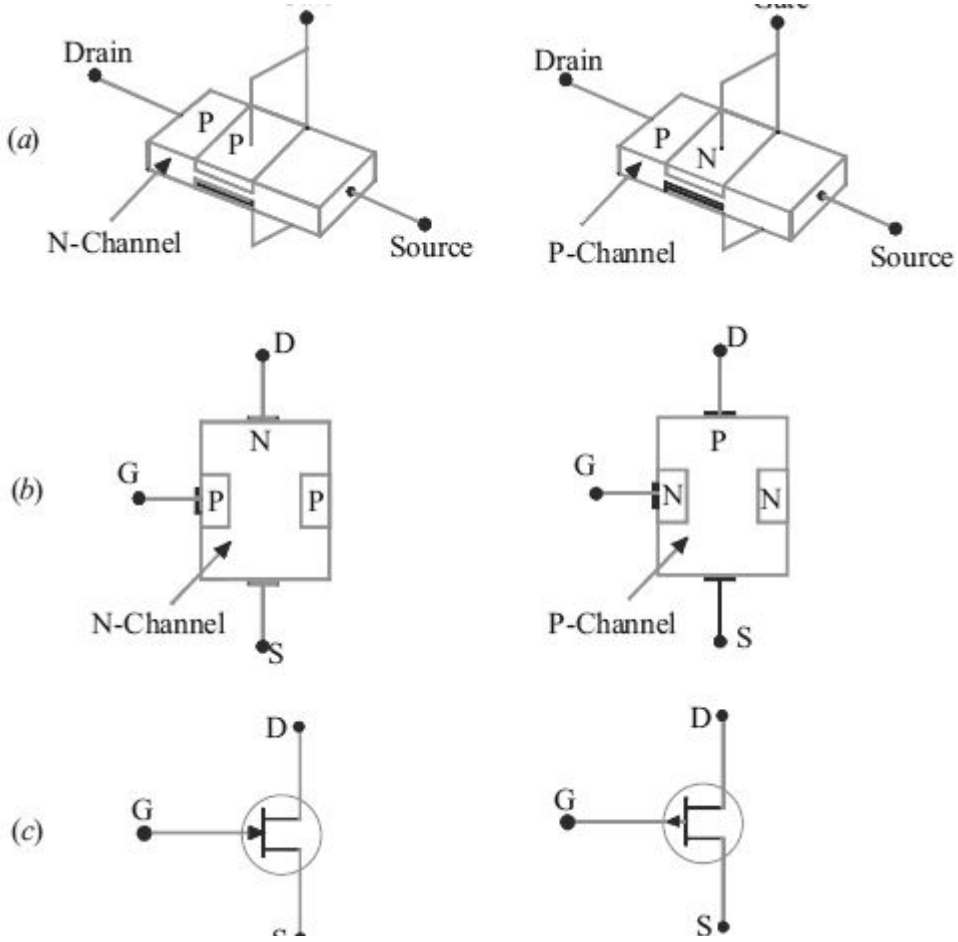


Fig. 1

Static Characteristics of a JFET

We will consider the following two characteristics:

(i) drain characteristic: It gives relation between ID and VDS for different values of VGS (which

is called running variable).

(ii) transfer characteristic: It gives relation between ID and VGS for different values of VDS.

We will analyze these characteristics for an N-channel JFET connected in the common-source

mode as shown in Fig. 2. We will first consider the drain characteristic when VGS= 0 and then

when VGS has any negative value upto VGS(off).

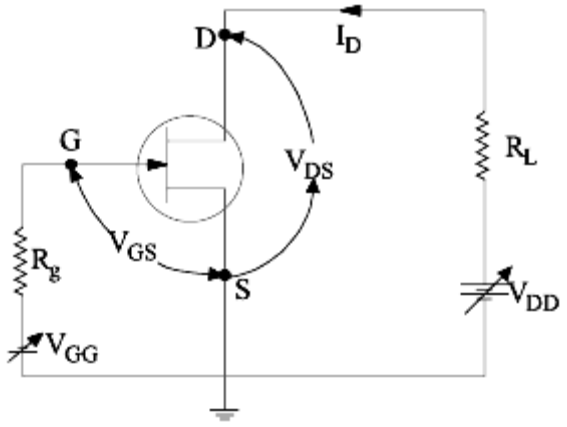


Fig. 2

JFET Drain Characteristic With $V_{GS} = 0$

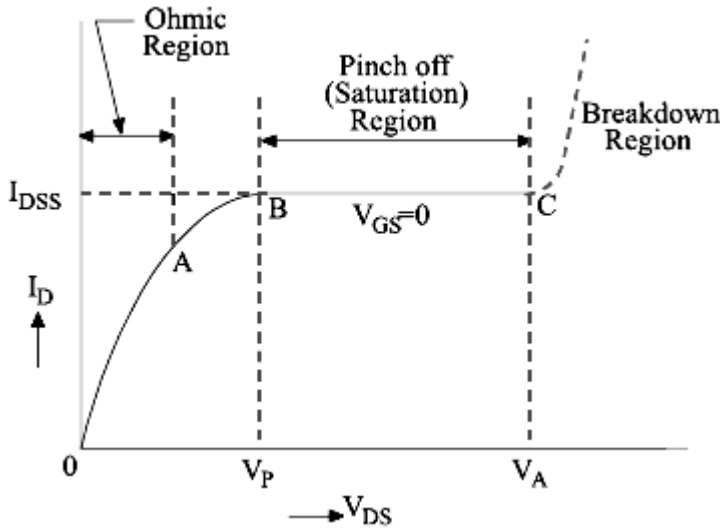
Such a characteristic is shown in Fig. 3.

It can be subdivided into following four regions :

1. Ohmic Region OA: This part of the characteristic is linear indicating that for low values of VDS, current varies directly with voltage following Ohm's Law. It means that JFET behaves like an ordinary resistor till point A (called knee) is reached.

2. Curve AB In this region, ID increases at reverse square-law rate upto point B which is called pinch-off point. This progressive decrease in the rate of increase of ID is caused by the square law increase in the depletion region at each gate upto point B where the two regions are closest without touching each other.

Fig.



3. Pinch-off Region BC: It is also known as saturation region or 'amplified' region. Here,

JFET operates as a constant-current device because ID is relatively independent of VDS. It is due to the fact that as VDS increases, channel resistance also increases proportionally thereby keeping ID practically constant at IDSS. It should also be noted that the reverse bias required by

the gate-channel junction is supplied entirely by the voltage drop across the channel resistance

due to flow of IDSS and none by external bias because VGS = 0.

4. Breakdown Region: If VDS is increased beyond its value corresponding to point C (called avalanche breakdown voltage), JFET enters the breakdown region where ID increases to an excessive value. This happens because the reverse-biased gate-channel P-N junction

undergoes avalanche breakdown when small changes in VDS produce very large changes in ID.

It is interesting to note that increasing values of VDS make a JFET behave first as a resistor (ohmic region), then as a constant-current source (pinch-off region) and finally, as a constantvoltage

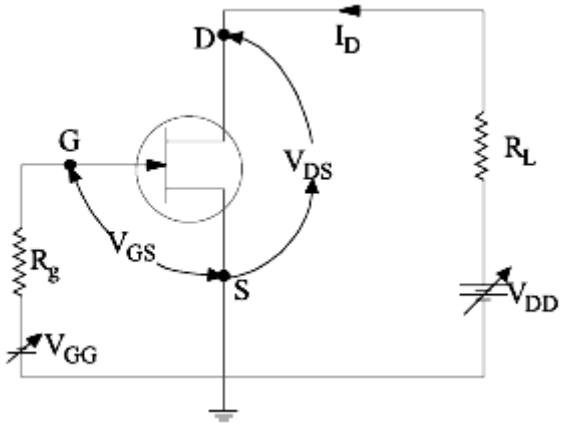
source (breakdown region).

Procedure :

1- Connect the circuit as shown in fig 4.

2- Let VDS =(0,0.5,1,1.5,2,2.5,3,4,5)v measure ID.

3- Repeat step 3 for VGS =(0.5,1,1.5,2,2.5,3,3.5,4,4.5) V.



Observation table

Conclusion:

College Name , City

Department of Electronics and Communication.

Electronic Devices and Circuit [EC – 303]

CHARACTERISTICS OF UNIJUNCTION TRANSISTOR

AIM:

To Plot and study the characteristics of UJT & determine it's intrinsic standoff Ratio.

APPARATUS REQUIRED:

S. No.	Name	Range	Type	Qty
1	R.P.S	(0-30)V		2
2	Ammeter	(0–30)mA		1
3	Voltmeter	(0–30)V		1
		(0–10)V		1

COMPONENTS REQUIRED:

S. No.	Name	Range	Type	Qty
1	UJT	2N2646		1
2	Resistor	1KΩ		2
3	Bread Board			1

THEORY:

UJT(Double base diode) consists of a bar of lightly doped n-type silicon with a small piece of heavily doped P type material joined to one side. It has got three terminals. They are Emitter(E), Base1(B1),Base2(B2).Since the silicon bar is lightly doped, it has a high resistance & can be represented as two resistors, r_{B1} & r_{B2}. When V_{B1B2} = 0, a small increase in V_E forward biases the emitter junction. The resultant plot of V_E & I_E is simply the characteristics of forward biased diode with resistance. Increasing V_{EB1} reduces the emitter junction reverse bias. When V_{EB1} = Vr_{B1} there is no forward or reverse bias. & I_E = 0. Increasing V_{EB1} beyond this point begins to forward bias the emitter junction. At the peak point, a small forward emitter current is flowing. This current is termed

as peak current(I_P). Until this point UJT is said to be operating in cutoff region.

When I_E increases beyond peak current the device enters the negative resistance region. In which the resistance r_{B1} falls rapidly & V_E falls to the valley voltage.Vv. At this point I_E = Iv. A further increase of I_E causes the device to enter the saturation region.

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set V_{B1B2} = 0V, vary V_{EB1} , & note down the readings of I_E & V_{EB1}
3. Set V_{B1B2} = 10V , vary V_{EB1} , & note down the readings of I_E & V_{EB1}
4. Plot the graph : I_E Versus V_{EB1} for constant V_{B1B2}.
5. Find the intrinsic standoff ratio.

FORMULA FOR INTRINSIC STANDOFF RATIO:

$\eta = V_P - V_D / V_{B1B2}$., where V_D = 0.7V.

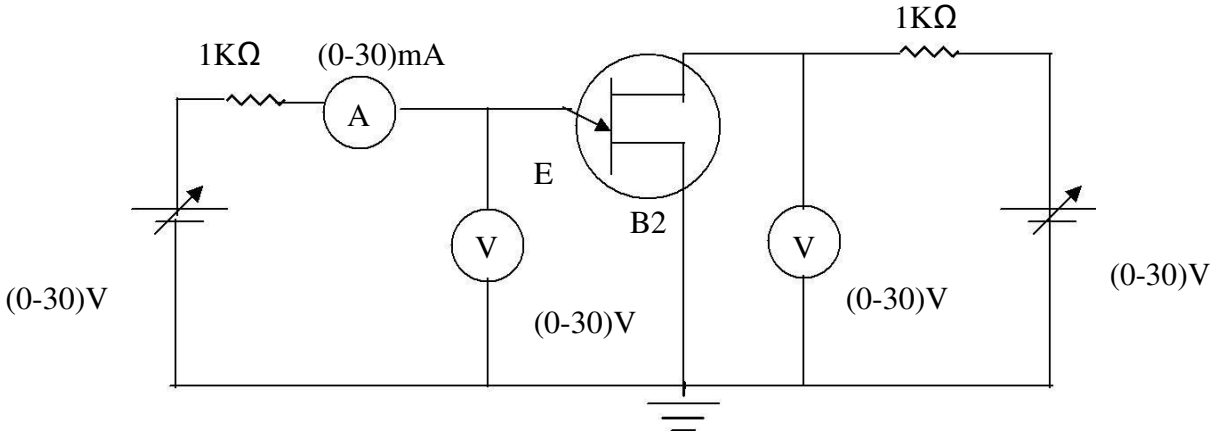
PROCEDURE:

1. Give the circuit connections as per the circuit diagram.
2. The dc input voltage is set to 20 V in RPS.
3. The output sweep waveform is measured using CRO.
4. The graph of output sweep waveform is plotted

RESULT:

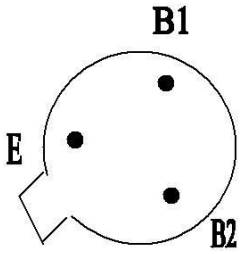
1. Thus the characteristics of given UJT was Plotted & its intrinsic standoff Ratio = ----.

CIRCUIT DIAGRAM:



PIN DIAGRAM:

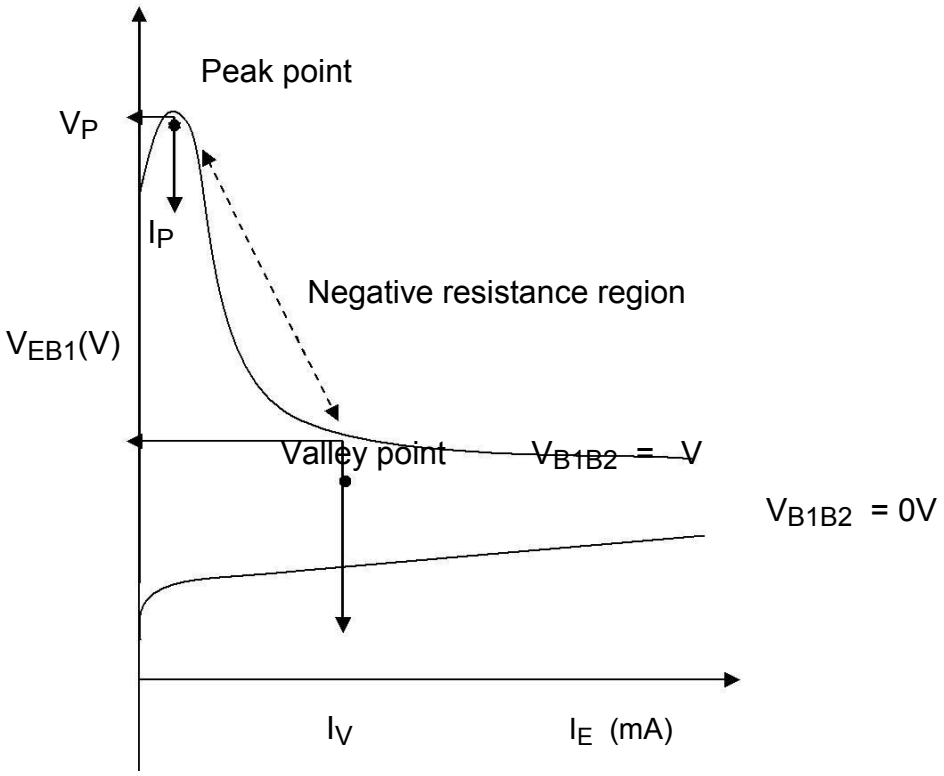
BOTTOM VIEW OF 2N2646:



SPECIFICATION FOR 2N2646:

* Inter base resistance R_{BB} = 4.7 to 9.1 KΩ
* Minimum Valley current = 4 mA
* Maximun Peak point emitter current 5 μA
*Maximum emitter reverse current 12 μA.

MODEL GRAPH:



TABULAR COLUMN:

V_{B1B2} = 0V		**V_{B1B2} = 10V**	
V_{EB1} (V)	**I_E (mA)**	**V_{EB1} (V)**	**I_E (mA)**