UNIT-4

1. Memory Hierarchy -
   - CPU
     - L1 cache
     - MMU
     - L2 cache
     - Memory
     - Disk
     - Virtual memory
   Run-time mapping from virtual to physical addresses is done by a hardware

3. Concept of memory management -
   - Functions of memory management -
     1. Keep track of the status of each memory location
     2. Determining allocation policy for memory
     3. Memory allocation technique, information must be updated
     4. Deallocation technique and policy
   - Requirement of memory management -
     1. Relocation
     2. Protection
     3. Sharing
     4. Logical organization
     5. Physical organization

2. MFT -> multiple contiguous fixed partition allocation (no longer used)
   MVT -> multiple contiguous variable partition allocation (dynamically allocated)

4. Logical address - an address generated by the CPU
   Physical address - one loaded into memory address register of the memory
   - Set of all logical addresses generated by a program is a logical address space
   - The set of all physical address corresponding to these logical addresses is a physical address space
Swapping -
A process, however, can be swapped temporarily out of memory to a backing store and then brought back into memory for continued execution. This is known as swapping, sometimes called page-out.

![Diagram]

Contiguous Memory Allocation -
Each process is contained in a single contiguous section of memory.

Dynamic Storage Allocation Problem Solution -
- *First Fit* - Allocate the first hole that is big enough.
- *Best Fit* - Allocate the smallest hole that is big enough.
- *Worst Fit* - Allocate the largest hole.

Fragmentation -
- External fragmentation - As processes are loaded and removed from memory, the free memory space is broken into little pieces. External fragmentation exists when there is enough total memory space to satisfy a request, but the available space is not contiguous.
- Internal fragmentation - Memory that is internal to a partition but is not being used.

Solution - Compaction, formats the logical address space of the processes to be noncontiguous.

Non-contiguous Memory Allocation -
Each process can have portions of processes distributed among many areas of memory.
PAGING -

It is a memory management scheme that permits the physical address space of a process to be a non-contiguous logical address.

```
CPU -> P | d
     |
     |   v
Page Table
     |
     |   v
Logical Memory
```

Physical Memory

```
Physical Address
0000...000
0111...111
```

PAGING HARDWARE

```
Page 0  0  1
Page 1  1  4
Page 2  2  3
Page 3  3  7
```

Page Table

```
Page Table
0  page 0
1  page 1
2  page 2
3  page 3
4  page 0
5  page 1
6  page 2
7  page 3
```

PAGING MODEL OF LOGICAL AND PHYSICAL MEMORY

```
Logical Address
m-n
```

```
Page Table Base Register (PTBR) points to the page table.
Translation Look-up Buffer (TLB) - special, small, fast-lookup hardware cache, high-speed memory.
Page Table Length Register (PTLR) indicate the size of the page table.
```

Basic Method -

Breaking physical memory into fixed sized blocks called frames & breaking logical memory into blocks of the same size called pages.

```
Page number | Page Offset
P | d
-> logical address space = 2^m
```

```
Page size = 2^n
```

8. Segmentation -
- It is a memory management scheme that supports linear addressing.
- Segment number \( \rightarrow \) offset \( \rightarrow \) logical address
- \( \text{limit} \rightarrow \) physical length of the image
- \( \text{page} \rightarrow \) starting physical address

9. Page combined with segmentation -
- To provide the efficiency of paging with the protection and sharing capabilities of segmentation.

10. Structure and implementation of page table -
- Hierarchical Paging -
  - page number, page offset
  - page table
  - page of the page table
- Hashed Page Table -
Hashed Page table - hash values being the virtual page number.

Inverted Page table - virtual address contains process id, page number, offset.

Concept of virtual memory - Virtual memory is a technique that allows the execution of processes that are not completely in memory.

Virtual address space of a process refers to the logical (or virtual) view of how a process is stored in memory.

Virtual address space that includes holes are known as sparse address space.

Cache memory organization -

Cache memory organization:

CPU → Cache → Main Memory

Demand Paging - A strategy is to initially load pages only as they are needed.

Pages is concerned with the individual pages of a program.

Effective access time = (1-p) × memory access time + p × page fault time

p → probability of a page fault.
Page Replacement Algorithms -
  → FIFO Page Replacement - first in first out
  → Belady’s Anomaly - For some page-replacement algorithms, the page fault rate may increase as the number of allocated frames is used for the longest period of time.
  → Optimal Page Replacement - Replace the page that will not be used for the longest period of time.
  → LRU Page Replacement - Least recently used.

Allocation of frames -
  → minimum no. of frames
  → Allocation algorithms -
    - Equal allocation - m frames among n processes
    - Proportional allocation - allocate available memory to processes according to its size
  → Global allocation - One process can take a frame from another
  → Local allocation - Each process selects from only its own set of allocated frames.

Thrashing - High page-out activity.
A process is thrashing if it is spending more time paging than executing.

Cores of thrashing - low CPU utilization
limits the effects of thrashing by a local replacement algorithm
  → Working set model - 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 (most recent page reference)
  → Working set window
    - Working set ∩ W.S.(t) = 8, 9, 10

To prevent thrashing - Page Fault Frequency - Page fault rate/number of frames.

Demand Segmentation - Used when insufficient hardware to implement demand paging.