### Evolution of Microprocessors

<table>
<thead>
<tr>
<th>Chip</th>
<th>Year</th>
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<tbody>
<tr>
<td>4004</td>
<td>1971</td>
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<tr>
<td>4040</td>
<td>1971</td>
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<tr>
<td>8008</td>
<td>1972</td>
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<tr>
<td>8080</td>
<td>1974</td>
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<td>8085</td>
<td>1976</td>
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<td>8086</td>
<td>1978</td>
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<td>8088</td>
<td>1979</td>
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<td>80286</td>
<td>1982</td>
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<tr>
<td>80386</td>
<td>1984</td>
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<tr>
<td>80486</td>
<td>1986</td>
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<tr>
<td>Pentium</td>
<td>1993</td>
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<tr>
<td>Pentium Pro</td>
<td>1995</td>
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<tr>
<td>Pentium 2</td>
<td>1996</td>
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<tr>
<td>Pentium 3</td>
<td>1998</td>
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<tr>
<td>Pentium 4</td>
<td>2000</td>
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<tr>
<td>Itanium 2 Duo</td>
<td>2004</td>
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<tr>
<td>Core i7</td>
<td>2008</td>
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<tr>
<td>Core i5</td>
<td>2009</td>
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<tr>
<td>Core i3</td>
<td>2010</td>
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### Microprocessor architecture and its operation

- Computer system consists of primary of:
  1. Microprocessor
  2. Memory
  3. Input
  4. Output

Internal logic design of the microprocessor called its architecture.

Microprocessor is programmable logic device designed with registers, flip-flops, and timing elements.
Microprocessor operations are -
(1) Microprocessor initiated operations
(2) Internal Data operations
(3) Peripheral (or externally) initiated operations

Microprocessor initiated operations -
→ Memory Read (Read data from memory)
→ Memory Writes (Write data into memory)
→ I/O Read (Accept data to output device)
→ I/O Writes (Send data to output device)

Internal Data Operations -
→ Store 8-bit data
→ Performed arithmetic and logical operations
→ Test for conditions
→ Sequence the execution of instructions
→ Store data temporarily during execution in the defined R/W memory locations called the stack.

Peripheral or Externally Initiated operations -
→ RESET (all internal operations are suspended and program counter is cleared)
→ Interrupt (execute "service routine" (emergency) instructions)
→ READY (low → MP enters into wait state)
→ Hold (MP relinquishes control bus and allows external peripheral to read

Memory -
(i) Primary Memory
   → ROM
   → ROM
   → Bipolar
   → Mask PROM
   → Mask PROM
   → EPROM
   → E-EPROM

(ii) Secondary Memory
   → Magnetic
   → Semiconductor
   → Static
   → Dynamic

only companion
2. **Input/Output (I/O)** -

Two different methods by which MPU identifies and communicates with I/O devices -

1. **Direct I/O (Peripheral)**
2. **Memory-mapped I/O**

<table>
<thead>
<tr>
<th>Direct I/O (Peripheral)</th>
<th>Memory-mapped I/O</th>
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<tbody>
<tr>
<td>→ 8 address lines to send the address of I/O device</td>
<td>→ 16 address lines to send the address of I/O device</td>
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<tr>
<td>→ Can identify $2^8 = 256$ input and output devices</td>
<td>→ Can identify $2^{16} = 64K$ input and output devices</td>
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<td>→ I/O Read (IOR) &amp; I/O Write (IOW) control signals used to enable the device</td>
<td>→ MENR and MENW control signals used to enable the device</td>
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</table>

3. **Data Transfer Scheme** -

Paralleled Data Transfer

1. Program controlled I/O or interrupt driven I/O polling control
2. Interrupt program controlled I/O or interrupt driven I/O
3. Hardware controlled I/O or DMA transfer
4. Handwritten I/O controlled by handshake signals
5. I/O controlled by ready signals

Program controlled I/O or polling control -

Data transfer is completely under the control of the microprocessor program. This means that the data transfer takes place only when an I/O transfer instruction is executed. In most of the cases it is necessary to check whether the device is ready for data transfer or not. To check this, microprocessor polls the status bit associated with the I/O device...
Interrupt-driven I/O -

When I/O data transfer is initiated by the external I/O device (i.e., device sends an interrupt signal to the microprocessor), the microprocessor stops the execution of the program and transfers the program control to an interrupt service routine. The interrupt service routine performs the data transfer. After the data transfer, it returns control to the main program at the point it was interrupted.

Hardware-controlled I/O - (increase the speed of data transfer)

In response of HBIB signal (sent by DMA controller to initiate data transfer), microprocessor releases its data, address, and control buses to the DMA controller.

I/O control by handshake signals -

The status of handshake signals are checked between the microprocessor and an I/O device, and when both are ready, the actual data is transferred.

I/O control by READY signal - (between slower I/O device and microprocessor)

If READY pin is high, the I/O device is ready for data transfer otherwise microprocessor enters WAIT state(s). Then WAIT state elongates the read/write cycle timings and prepare microprocessor to communicate with slower I/O devices.

6. Interfacing Devices -

Interfacing the processor with one or more peripheral devices for the purpose of communication with the environment.

Tri-state device -

It has three states (Logic 1, Logic 0 and high impedance)

\[ I/O \rightarrow O/P \]

Enable/Disable
Branch - It is a logic circuit that identifies each combination of the signals present at its input.

Latch - A latch is a D-flip-flop, used commonly to interface output device.

Gate, shift registers and buffers are also an interfacing devices.

7. Architectural Advancements of microprocessors
   - Memory Management, Multitasking, pipelining, multiprogramming and virtual memory are main architectural advent advancements of microprocessors.

8. Microprocessor development systems -
   - It is a tool that allows the designer to develop, debug and integrate error-free application software in microprocessor system.
   - It falls into two categories -
     1. Non-universal systems (Intel, Motorola, RCA)
     2. Universal systems (Hewlett-Packard, Tektronix)

**Typical microprocessors** - Intel 8086/MP and Motorola MC

Microprocessors are being extensively used in wide variety of applications. Typical application includes dedicated controlling, personal workstations, and real-time robotics control.