**UNIT IV**

Communication & Bus Interfacing with 8085/8086 Microcontroller

I/O and Memory Interfacing using 8085/8086

I/O and Memory Interfacing using 8085/8086

1. **Memory Interfacing**
   - Memory Organization
   - Memory map, Address decoding

2. **Memory Interfacing to Microprocessor**

3. **Interrupts of 8085 Microcontroller**
   - INTR → Interrupt Request
   - RST 5.5 → 002H Address
   - RST 6.5 → 003H Address
   - RST 7.5 → 003CH Address
   - TRAP → Non-maskable interrupt (Used for power failure or emergency shut down)

- **RIIM Instruction** - (Read Interrupt Mask) → load accumulator with 8-bit
  - SIO P7 P6 P5 P4 IE M7 M6 M5 M4

- **SIIM Instruction** - (Set Interrupt Mask) → load accumulator with
  - LSD SDE XXX R7 R6 R5 R4 R3 R2 R1 R0
  - MSE → Mask set enable, SDE → Serial Data Enable
(3) **Interrupts of 8086 microprocessor**

(I) **Software Interrupts**
- 256 Interrupts from INT 00H to INT 0FH
  - **Interrupt Type 0** - INT 00H → **Divide by zero error**
  - **Interrupt Type 1** - INT 01H → **Single step**
  - **Interrupt Type 2** - INT 02H → **Non maskable Interrupt**
  - **Interrupt Type 3** - INT 03H → **Break point**
  - **Interrupt Type 4** - INT 04H → **Overflow Interrupt**
  - **INT 05H to INT 07H** → Reserved
  - **INT 08H to INT 0FH** → User defined

(2) **INT INTerrupt** - Type 0 to 255

When IF is set, INT R input is enabled

(3) **External Hardware interrupt interface with 8086 CPU**

![Diagram of interrupt interface]

(4) **Priority of 8086 Interrupts**

- **Result**
  - **Internal Interrupts**
  - **Software Interrupts**
  - **Nonmaskable Interrupts**
  - **Hardware Interrupts**

(5) **Interrupt Instructions of 8086**
- **CLI** (Clear Interrupt Instruction)
- **STI** (Set Interrupt flag), **IRET** (Interrupt Return), **INTO** (Interrupt overflow), **HLT**, **WAIT**
8259A Programmable Interrupt Controller (PIC) — [28 pins]

Architecture:

- Data Bus
- Control Logic
- Interrupt Request Register (IRR)
- Interrupt Mask Register (IMR)
- IR0, IR1, IR2, IR3
- INTR, INTE
- CS
- CAS
- CAS1
- CAS2
- Cascade Lines
- 8259A
- SPIEN
- IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, IRQ5

Interfacing of 8259A with 8085

Address Bus

Control Bus

Data Bus

Two types of Command Words:

- Initial Command words (ICWs) and Operation command words (OCWs)
- Four types (ICW1, ICW2, ICW3, ICW4) with three types (OCW0, OCW2, and OCW4)

Always read in cascade mode operations.
8255A Programmable Peripheral Interface (PPI) - [50 mins]

Architecture:

- **GROUP A**
  - CONTROL
  - PORT A (8)

- **GROUP A**
  - PORT C
  - UPPER (4)
  - PORT B
  - LOWER (4)

- **GROUP B**
  - PORT C
  - (3)
  - PORT B
  - (8)

**Control Word**:
- If $D_7 = 0$ then BSR mode (Single-I/O mode)
- If $D_7 = 1$ then I/O mode (Mode 0, Mode 1 and Mode 2)

**I/O Mode**:
- $D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0$

- **PORT A**
  - $1$: INPUT
  - $0$: OUTPUT

- **PORT B**
  - $1$: INPUT
  - $0$: OUTPUT

- **PORT C (LOWER)**
  - $1$: INPUT
  - $0$: OUTPUT

- **PORT C (UPPER)**
  - $1$: INPUT
  - $0$: OUTPUT

**Mode Set Flag**
- $1$: ACTIVE

- **Mode Selection**
  - $00$: Mode 0
  - $01$: Mode 1
  - $1x$: Mode 2
### Operation Modes

1. **Mode 0 (Basic I/O)** - Simple I/O for port A, B, and C.
2. **Mode 1 (Strobed I/O)** - Simple I/O for port A and B. Port C can be used as control signals for handshaking.
3. **Mode 2 (Bi-directional I/O)** - Bi-directional bus for port A & B. Port C can be used in either Mode 1 or Mode 0. Port C can be used as control signals for handshaking.

### Single-bit Set/Reset (BSR) Mode

Eight bit of Port C can be set or reset using a single output instruction.

### Applications of PPI

Putting on LED as specified by the designer, generating a square wave at port A, Interfacing A/D Converter, keystroked operation, sequential pulsing of lights, Traffic light control.
8253 Programmable Counter/Interval Timer

- **CS**
  - **A<sub>3</sub>**
  - **A<sub>0</sub>**
  - **SELECTION**
    - 0 0 0: COUNTER 0
    - 0 0 1: COUNTER 1
    - 0 1 0: COUNTER 2
    - 0 1 1: NO OPERATION
  - 1 1 X: 8253 IS NOT SELECTED

**Control Word Register**

- **SC<sub>1</sub>**
- **SC<sub>0</sub>**
- **Ra<sub>1</sub>**
- **Ra<sub>0**
- **M<sub>2</sub>**
- **M<sub>1</sub>**
- **M<sub>0**
- **BCD**

**SC (Select Counter)**

- 0 0: COUNTER 0
- 0 1: COUNTER 1
- 1 0: COUNTER 2
- 1 1: ILLEGAL

**M (Mode)**

- 0 0 0: MODE 0
- 0 0 1: MODE 1
- 0 1 X: MODE 2
- 1 0 X: MODE 3
- 1 1 0: MODE 4
- 1 1 1: MODE 5

**BCD**

- 0 → Binary Counter (16 kHz)
- 1 → Binary Coded Decimal (BCD) counter (4 decades)
### RL (Read/Load)

<table>
<thead>
<tr>
<th>RL₂</th>
<th>RL₀</th>
<th>READ/LOAD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Counting Operation</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Read/Load least significant byte only</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Read/Load most significant byte only</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Read/Load least significant byte first, then most significant byte</td>
</tr>
</tbody>
</table>

**MODE 0** - Interrupt on Terminal Count (GATE = 1)

- **MODE 1** - Programmable one shot (GATE = 0 half + 1 1/2 1/2 half = 0)
- **MODE 2** - Rate Generator (OUTPUT = 1 for (N-1) pulses)
- **MODE 3** - Square-wave Generator (of N-1 even, OUT = 1 1/2 half + 1/2 1/2 half = 0)
  - If N is even, high for N/2 pulses and low for next N/2 clock pulses.
  - If N is odd, output high for N+1 pulses and low for remaining clock pulses.
- **MODE 4** - Software Triggered Mode (GATE = 1, OUT = 1 for N-1 then one low pulse and then again OUT = 1 for N and 0 m)
- **MODE 5** - Hardware Triggered Mode (whenever GATE = 1 then it starts counting clock like MODE 4)

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### Communication and Bus Interfacing with 8085/8086 Microprocessor

**Serial Communication Interface 8251 - [28 pins] (USART)**

A

<table>
<thead>
<tr>
<th>Asynchronous Data Transfer</th>
<th>Synchronous Data Transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) Start bit and stop bit is required</td>
<td>(c) No need: clock header is used</td>
</tr>
<tr>
<td>(b) Low-speed data transfer</td>
<td>(e) High-speed data transfer</td>
</tr>
<tr>
<td>(d) Transmitter need not to be synchronized</td>
<td>(f) Transmitter is synchronized with the receiver</td>
</tr>
<tr>
<td>(g) Data can be sent one character at a time</td>
<td>(h) Data can be sent one character at a time</td>
</tr>
<tr>
<td>(i) It can be implemented by hardware and software</td>
<td>(j) It can be implemented by hardware only</td>
</tr>
<tr>
<td>(k) Used to for transferring large amount of data</td>
<td></td>
</tr>
</tbody>
</table>
DSR → Data Set Ready, DTR → Data Terminal Ready
CTS → Clear to Send, RTS → Request to Send
SYNDET/BD → Synchronous Detect / Break Detect

Interfacing of 8251 with microprocessor:

Two function types:

(1) Mode Instruction Control Word -

<table>
<thead>
<tr>
<th>Bit Selection</th>
<th>S2</th>
<th>S1</th>
<th>EP</th>
<th>PEN</th>
<th>L2</th>
<th>L1</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invalid</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1st</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1 1/2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2nd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- 5 bits
- 6 bits
- 7 bits
- 8 bits

<table>
<thead>
<tr>
<th>Band Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>1x Asynch</td>
</tr>
<tr>
<td>16x Async</td>
</tr>
<tr>
<td>64x Async</td>
</tr>
</tbody>
</table>
(2) Command Instruction Words -

<table>
<thead>
<tr>
<th>D1</th>
<th>EH</th>
<th>IR</th>
<th>RTS</th>
<th>E.R</th>
<th>SBRK</th>
<th>RXE</th>
<th>DTR</th>
<th>TXEN</th>
</tr>
</thead>
</table>

TXEN → Transmit Enable → 1, Disable → 0
DTR → Data Terminal Read, DTR = 0
RXE → Receive Enable → 1, Disable → 0
SBRK → Send Break Character
E.R → Request Error flags
RTS → Request to Send
IR → Internal Reset
EH → Hunt for sync character

8 Direct Memory Access (DMA) Controller 8257 - [40 Pins]

Terminal Count Register (Tc) → (16 bit register)
Store heartbeats which will be transmitted through a DMA channel.
**Mode 1st Register**

- Mode 1
- Mode 0
- Extended WR
- Rotate Pair

**Status Register**

- Update Flag
- TSC0
- TSC1
- TSC2

**Interfacing of 8257 with 8085 microcontroller**

- **Data Bus**
- **Address Bus**
- **Control Lines**

**In master mode operation**

- **MEMR**
- **MEMW**
- **A0-A7**
- **A8-A15**

**In slave mode operation**

- **DATA BUS**
- **A0-A15**
- **A8-A15**
- **A0-A7**
- **HLDA**
- **8257**
- **DRQ**
- **DACK**
8279 - Programmable Keyboard and Display I/O Interface

- Input (Keyboard) Modes:
  - Scanned Keyboard
  - Scanned Sensor Matrix
  - Mixed Input
- Output (Display) Modes:
  - Display mode
  - Display entry
- Interfacing 8279 with microcontroller

Diagram:

- Status
- FIFO/SENSOR RAM
- Data Buffer
- Control and Timing Register
- 16x8 Display RAM
- Scanner Counter
- SCAN
- DATA
- BUS
- 8-bit Address
- Data Bus
- Control
- DATA
- ADDR
- DISPLAY ADDRESS REGISTERS
- Display Register
- OUTB3-OUTB0
- OUTA3-OUTA0
- 40 pins (Control/Interface I/O)}
Keyboard Interface of 8279

- IRQ
- DATA BUS
- WR
- RD
- RESET
- CLK
- SHIFT
- CNTL

64 Key Keyboard
R1o - R16 → Column lines
Decoder without line - row lines
256 functions

Sixteen digit display interface with 8279

<table>
<thead>
<tr>
<th>16 Nos. of display</th>
<th>S0</th>
<th></th>
<th></th>
<th></th>
<th>4 line to 16 line decoder</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>S1</td>
<td>S2</td>
<td>S3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
</tr>
</tbody>
</table>

\[ A0 - A3 \]
\[ B0 - B3 \]
\[ BO \] → Blank display
Bus Interface:
- Different types of data transfer:
  - Memory devices to CPU
  - CPU to memory devices
  - I/O devices to CPU
  - CPU to I/O devices
  - I/O devices to or from memory
A bus is a communication pathway that connects CPU, memory, and I/O.

Bus Structure of a microcomputer:

- ISA (Industry Standard Architecture) → by IBM in 1979
- EISA (Extended ISA) → by HP, AT&T, Compaq in 1987
- MCA (Micro Channel Architecture) → by IBM in 1987
- VESA (Video electronic standard association) → developed in 1980
- PCI (Peripheral Component Interconnect) → by Intel in 1993
- ACP (Accelerated Graphics Port) → by Intel in 1998
- USB (Universal Serial Bus) → by group of companies in mid 1990s
- Parallel Printer Interface → by IBM in 1981
- RS-232C → by EIA in 1960s
- IEEE - 488 Bus → General Purpose Interface Bus (GPIB) by HP
1. 8089 I/O processor

   - CPU
   - MAIN CONTROL
   - ALU
   - CHANNEL CONTROL
   - REGISTER FILE
   - DMA REQUEST
   - DMA TERMINATE

   STATUS
   BUS CONTROL AND ARBITRATION
   ADDRESS / DATA BUS

   - I/O BUS

   - I/O CHANNEL 1
   - I/O CHANNEL 2

   ASSEMBLY
   INSTRUCTION FETCH UNIT

   - CHANNEL CONTROL
   - REGISTER FILE
   - DMA TERMINATE

Applications:
- File management in hard disk and floppy disk
- Soft error recovery routine and error control
- CRT control (cursor control and auto scrolling)
- Keyboard control
- Communication control
- General I/O applications