PIPELINE PROCESSOR

1. Serial Pipeline Processor -
   A sequence of sub-tasks with serial precedence.

   ![Serial Pipeline Diagram]

   Synchronous model -

   ![Synchronous Model Diagram]

   Speedup = \( \frac{nK}{K+n-1} \)

   Efficiency = \( \frac{n}{k+n-1} \)

   Throughput = \( \frac{Nf}{K+n-1} \)

2. Non-serial Pipeline Processor -

   ![Non-serial Pipeline Diagram]

   Three stage pipeline

   Reservation table - show the path of data flow in pipeline

   Latency → No. of time units between two initiations of a pipeline

   Collision vector, state diagram, MA2 (Maximum Average latency)

   Speedy cycle, average latency

3. Instruction Pipeline design

   → Instruction execution phases -

   (1) Instruction fetch
   (2) Decode
   (3) Operand fetch
   (4) Execute
   (5) Write back phase
ILP → Instruction level parallelism

→ Mechanism for instruction pipeline -
  → Pre-fetch buffers -
    (1) Sequential buffers
    (2) Target buffers
    (3) Work buffers

→ Internal data forwarding -
  (1) Store-Store (STO)
  (2) Store-Load (MOVE)
  (3) Load-Load (MOVE)

Pipe/line Hazards -
(1) Structural Hazards
  (2) Data Hazards (RAW, WAW, WAR Hazards)
  (3) Control Hazards

Dynamic Instruction scheduling -
(1) Static - window
(2) Tomasulo algorithm

Branch Handling Techniques -
(1) Bit Dynamic Branch Prediction
(2) Branch Target Buffers
(3) Delayed Branch

Arithmetic Pipeline design -
(1) Static arithmetic pipeline (fixed + operation)
(2) Multifunctional arithmetic pipeline (more than one ALU operation)

Superscalar Pipeline design - m instruction issue rate, m ILP to fully utilize the pipeline

Superpipeline processor design -