

## UNIT – 3

### Sequential Circuits

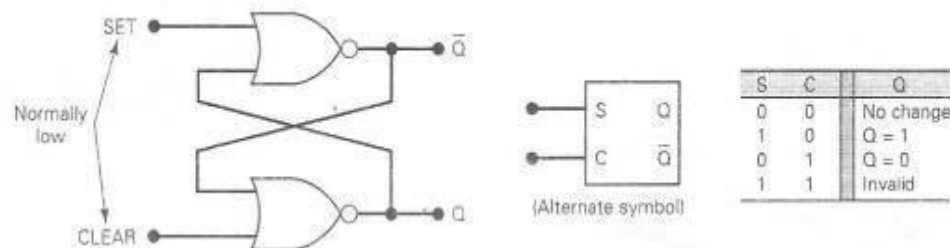
#### Unit-03/Lecture-01

#### Introduction

#### Sequential Circuits:

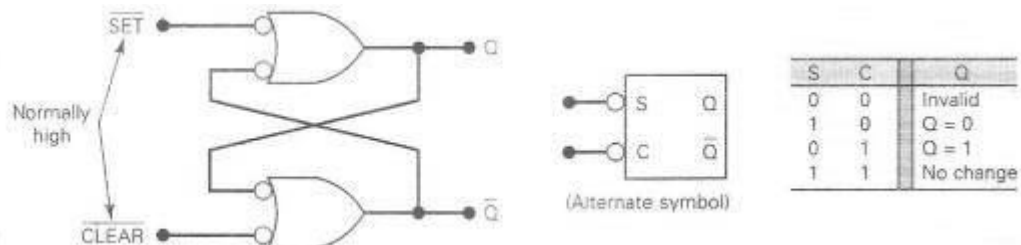
- The timing parameter comes into picture
- The output depends on the present time inputs, the previous time inputs, the previous output and the sequence in which the inputs are applied
- In order to provide the previous inputs or outputs, a memory element is required to be used. Thus it has a memory element.
- A memory element is as shown below:

NOR Latch

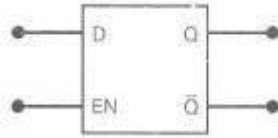


- Present State:  $Q_n$ , The data stored by the memory element at any instant of time is called the present state. The state prior to the application of the clock pulse
- Next State :  $Q_{n+1}$ , The circuit operates on the external inputs and the present state to produce new outputs. Some of these new outputs are stored in the memory element and called as the next state of the sequential circuit. The state after the application of the clock pulse.

NAND Latch



D Latch



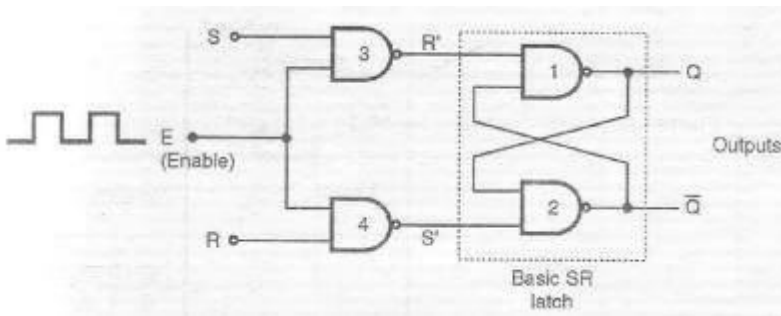
EN	D	Q*
0	X	No change
1	0	0
1	1	1

\*Q follows D input  
while EN is HIGH

## Unit-03/Lecture-02

### Flip Flops

#### SR or SC Flip Flop



1.  $E=0$ , FF3,4 forced = 1 irrespective of values or SR.
2.  $E=1, S=R=0$ , FF3,4 forced = 1, NO change
3.  $E=1, S=0, R=1$ , Reset condition
4.  $E=1, S=1, R=0$ , Set condition
5.  $E=1, S=1, R=1$ , Race around condition, to be avoided

Inputs				Outputs		Comments
Case	Enable E	S	R	$Q_{n+1}$	$\bar{Q}_{n+1}$	
I	0	x	x	$Q_n$	$\bar{Q}_n$	No change as $E = 0$
II	1	0	0	$Q_n$	$\bar{Q}_n$	No change (NC)
III	1	0	1	0	1	Reset condition
IV	1	1	0	1	0	Set condition
V	1	1	1	Indeterminate		Avoid this condition

#### FF SR TT

CLK	$S_n$	$R_n$	$Q_{n+1}$	$\bar{Q}_{n+1}$
↑	0	0	$Q_n$	$\bar{Q}_n$
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	Race	Race

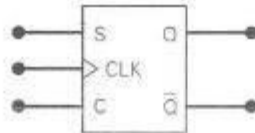
#### Excitation Table:

- When the present and next state of a circuit is given and we are expected to find the corresponding input condition then Excitation Table.

### FF SR ET(Excitation Table)

Present state of Q output	Next state of Q output	$S_n$ input	$R_n$ input
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Clocked S-C

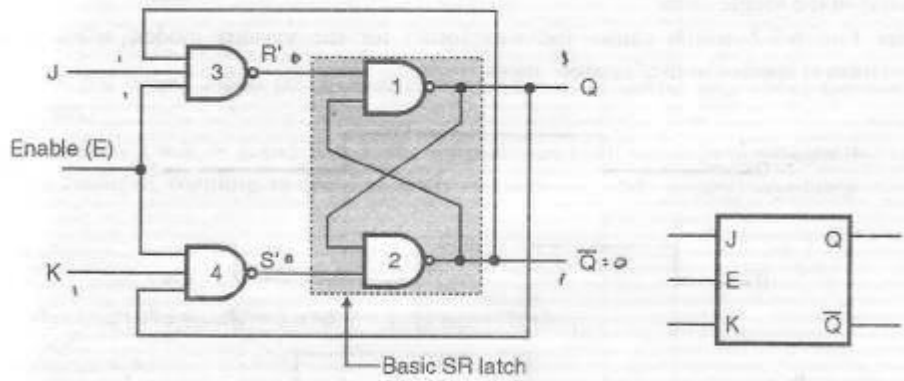


S	C	CLK	Q
0	0	↑	$Q_0$ (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

↓ of CLK has no effect on Q

## Unit-03/Lecture-03

### JK Flip Flop



- Operation of the JK FF is exactly the same as that of SR FF mentioned above but in addition avoids the Race around Condition.

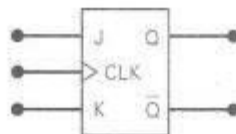
Inputs			Outputs		State
E	J	K	$Q_{n+1}$	$\bar{Q}_{n+1}$	
0	x	x	$Q_n$	$\bar{Q}_n$	No change
1	0	0	$Q_n$	$\bar{Q}_n$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	$\bar{Q}_n$	$Q_n$	Toggle

### FF JK ET(Excitation Table)

Q output		Inputs	
Present state	Next state	$J_n$	$K_n$
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Don't care conditions result due to toggling

Clocked J-K



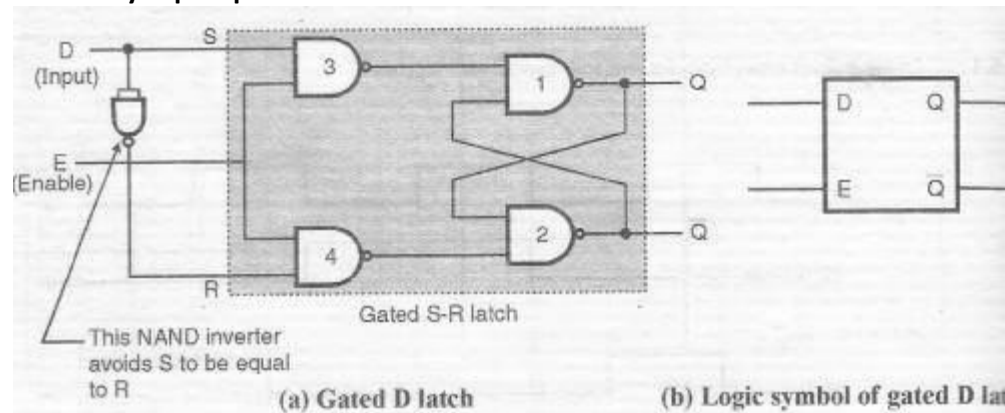
J	K	CLK	Q
0	0	↑	$Q_0$ (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\bar{Q}_0$ (toggles)

↓ of CLK has no effect on Q

S.NO	RGPV QUESTIONS	Year	Marks
Q.3	Explain the Operation of JK FF	Jun 05	10
Q	What is meant by Race Around Condition how it is avoided?	Jun 05	4

## Unit-03/Lecture-04

### D or Delay Flip Flop



The D FF is called the Delay FF as the output is same as the input but appears after the clock pulse.

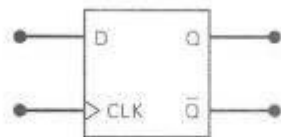
Rest of the operation is same as the JK FF because it is a JK FF with one of the inputs is connected the other with the help of a NOT Gate.

Inputs		Outputs		Comment
E	D	$Q_{n+1}$	$\bar{Q}_{n+1}$	
0	x	$Q_n$	$\bar{Q}_n$	No change (NC)
1	0	0	1	Reset condition
1	1	1	0	Set condition

### FF D ET(Excitation Table)

Q output		Input
Present state	Next state	
0	0	0
0	1	1
1	0	0
1	1	1

Clocked D

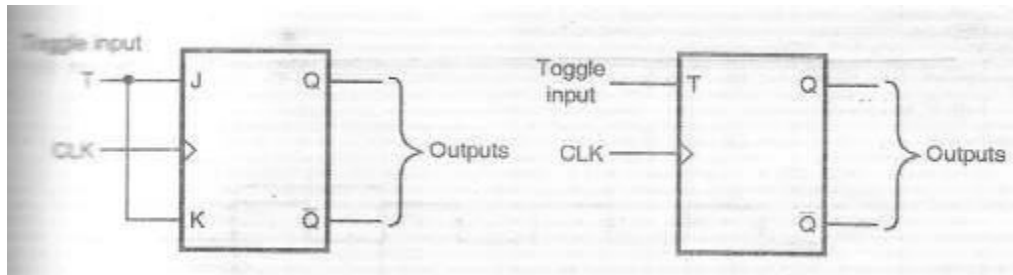


D	CLK	Q
0	↑	0
1	↑	1

↓ of CLK has no effect on Q

## Unit-03/Lecture-06

### T or Toggle Flip Flop



T is called the Toggle FF as the outputs toggle i.e. change from 0 to 1 or 1 to 0 after the application of the clock pulse. It is a JK FF with both the inputs tied together.

Inputs		Outputs		State
CLK	T	$Q_{n+1}$	$\bar{Q}_{n+1}$	
↑	0	$Q_n$	$\bar{Q}_n$	No change
↓	x	$Q_n$	$\bar{Q}_n$	No change
1	x	$Q_n$	$\bar{Q}_n$	No change
0	x	$Q_n$	$\bar{Q}_n$	No change
↑	1	$\bar{Q}_n$	$Q_n$	Toggle

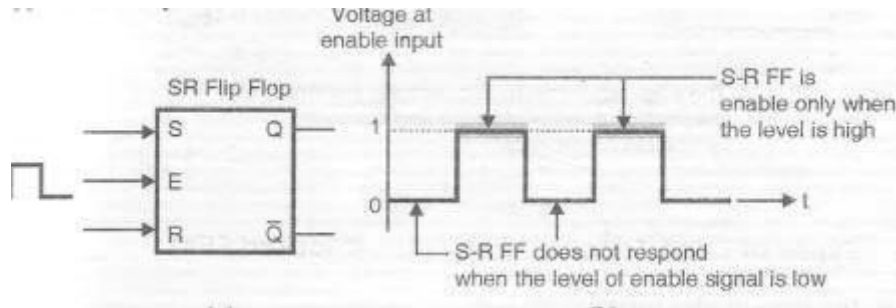
**FF T ET (Excitation Table)**

Q output		Input
Present state	Next state	
0	0	0
0	1	1
1	0	1
1	1	0

## Unit-03/Lecture-07

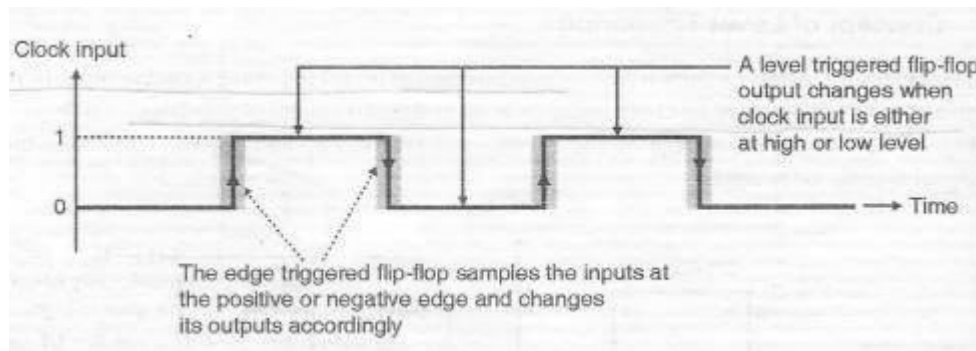
### Clocked and Edge Triggered

- The Latch or FF circuits which respond to their inputs, only if their enable input  $E$  held at an active HIGH or LOW level are called Level Triggered latches for FF.
- They can be of two types
- Positive Level – The output responds when the clock input is HIGH (1)
- Negative Level - The output responds when the clock input is LOW (0)



### Edge Triggered

- The FF changes their output corresponding to the positive or negative edge of the clock input.
- Can be of two types
- Positive Edge Triggered: Change when the positive going edge (0-1)
- Negative Edge Triggered: Change when the negative going edge (1-0)





## Unit-03/Lecture-08

- Flip Flop is a 1 bit memory cell which can be used for storing the digital data.
- To increase the storage capacity in terms of number of bits, we use group of FFs called Registers
- Data in serial form is called **Temporal Code** and Parallel form is called **Special Code**

Registers are classified as

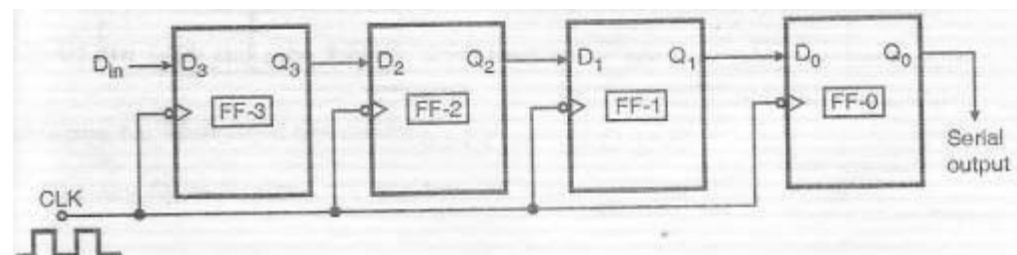
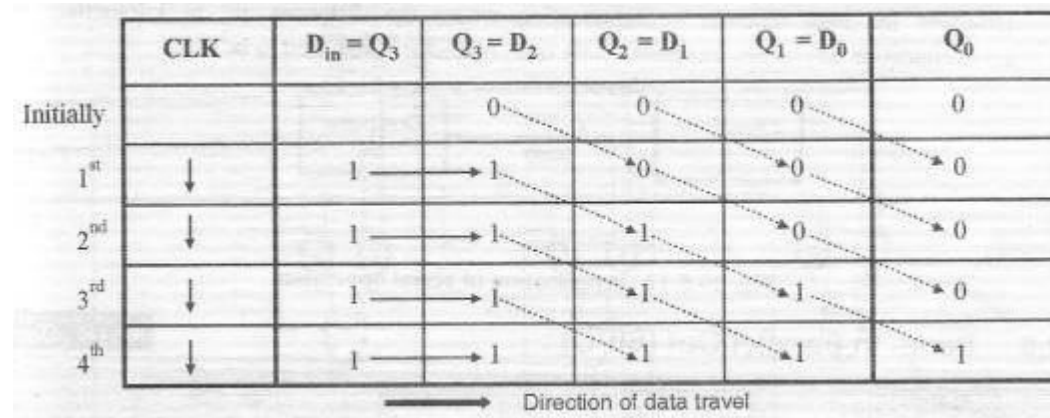
1. SISO – Serial In Serial Out
2. SIPO – Serial In Parallel Out
3. PISO – Parallel In Serial Out
4. PIPO – Parallel In Parallel Out

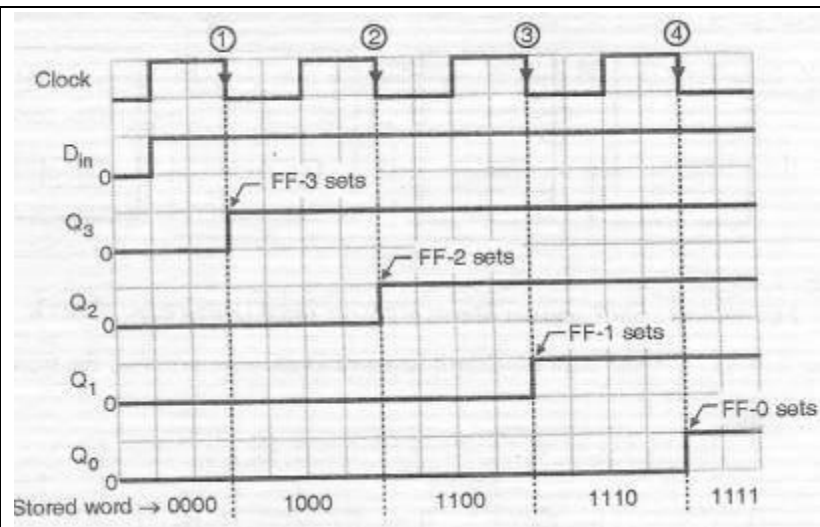
### Shift Registers

- The binary data in a register can be moved within the register from one FF other or outside it with application of clock pulses
- The register that follows such data transfers are called as **Shift Registers**.
- Shift Registers are used for Data Storage, Data Transfer, Certain arithmetic and Logic Operations.

### Shift Registers – SISO

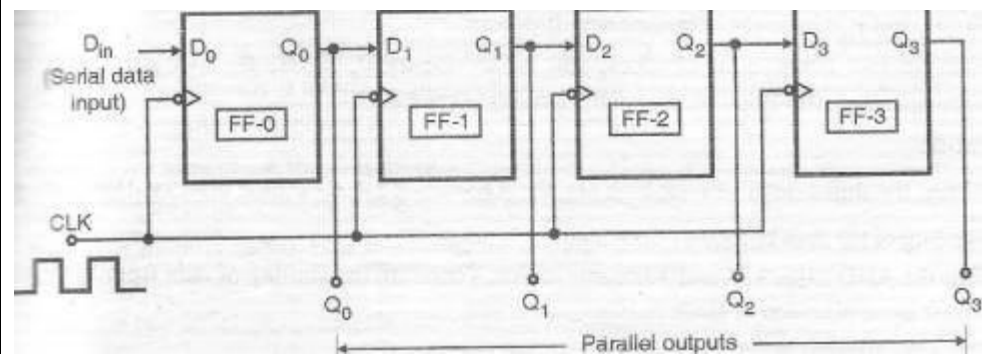
Data Bits shift from left to right by 1 position per clock cycle.





## SIPO

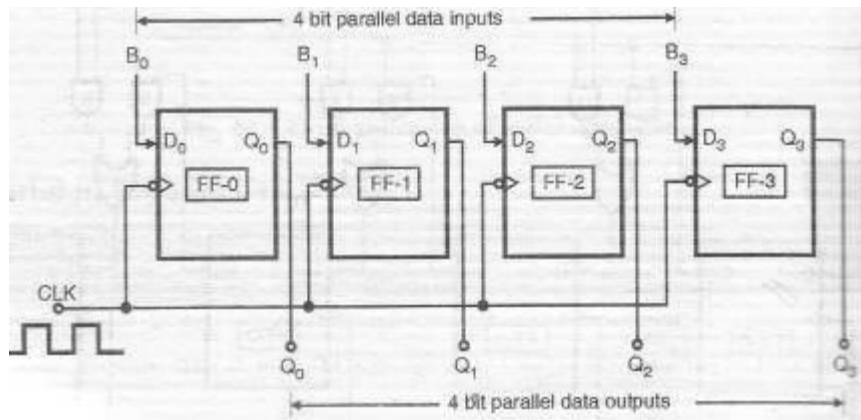
All output are made available simultaneously after 4 clock pulses.



## Unit-03/Lecture-09

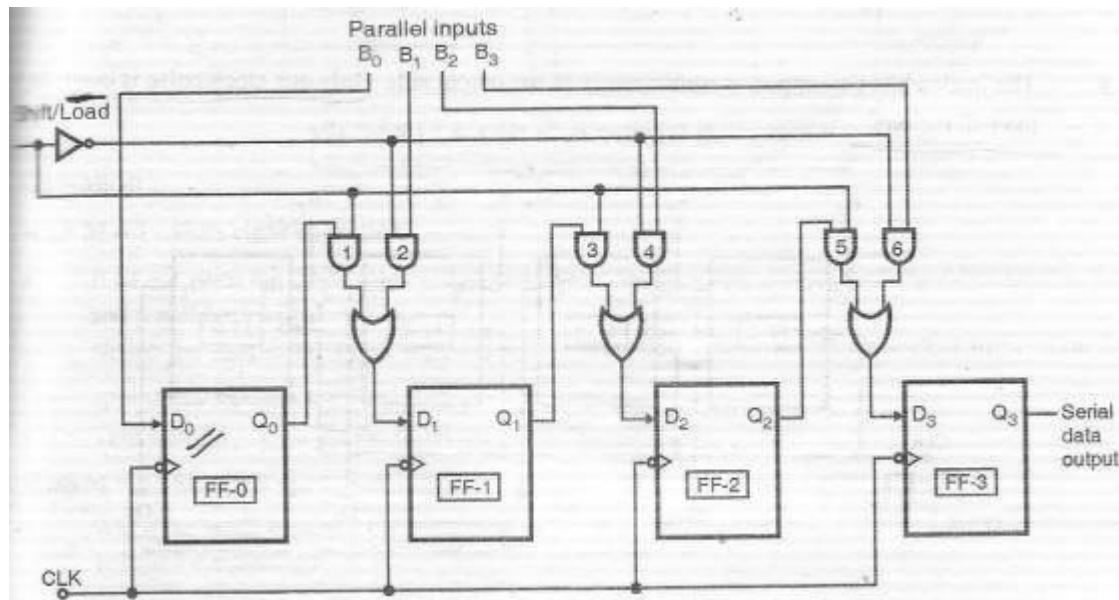
### PIPO

All the inputs are loaded simultaneously and are available simultaneously after the application of the clock pulse.



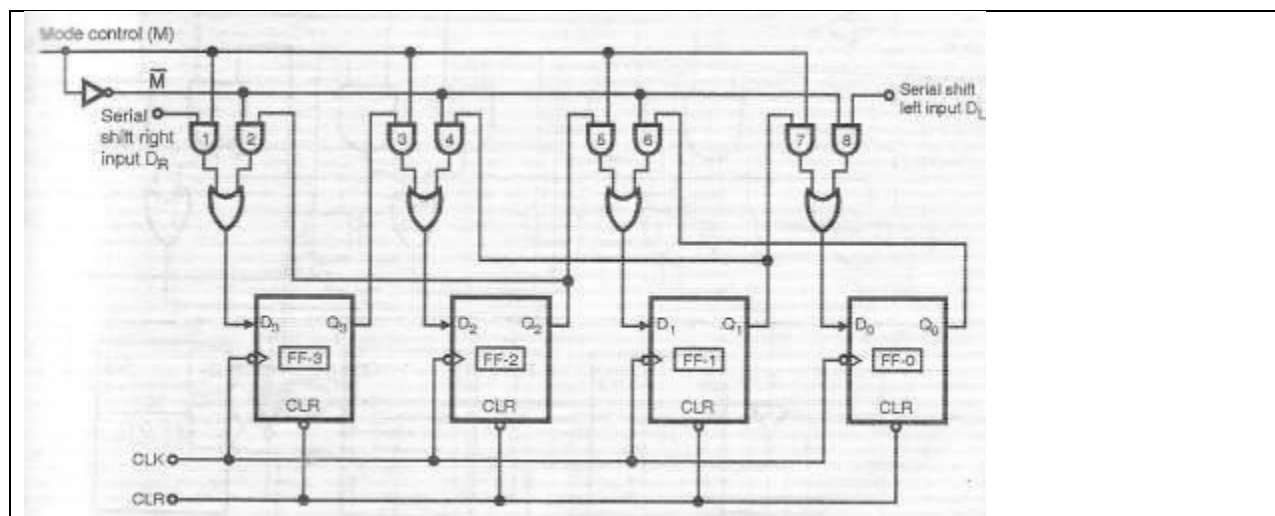
### PISO

All Inputs are loaded simultaneously but output is bit wise.



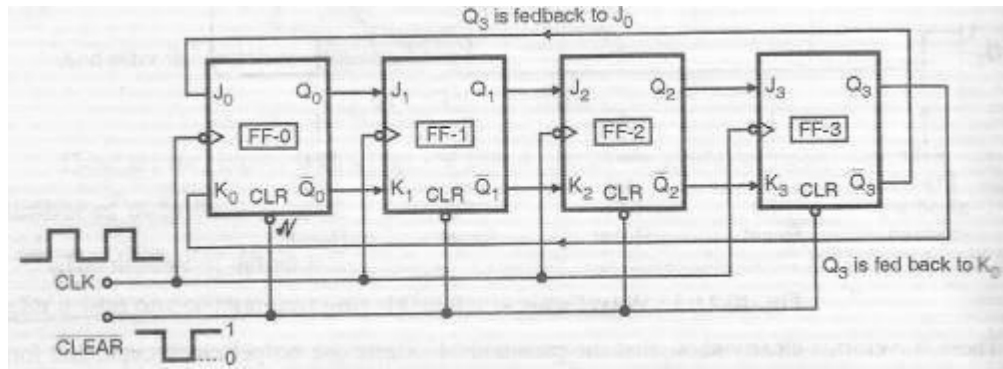
### Bidirectional Shift Register

- Shift Left is equivalent to multiplying and shift Right is to division by 2 respectively.
- Such a register is called the bidirectional register.
- There are two serial inputs DR(Right) and DL (Left) along with the mode select input M



## Unit-03/Lecture-10

### Johnsons Counters



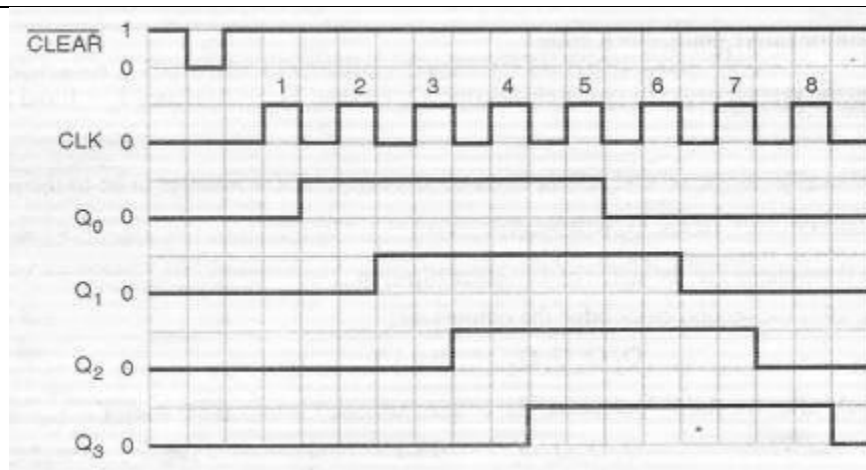
#### Operation;

- Clear operation sets All outputs to 0000
- After application of 1<sup>st</sup> negative edge clock pulse  
Outputs will change to 0001 as FF0 will set while rest will have no change.
- $Q_3=0$ ,  $Q_3'=1$ , Hence  $J_0=1, K_0=1$ , also  $Q_0=1$  hence  $J_1=1$  After application of 2<sup>nd</sup> negative edge clock pulse. FF0 continues to be in set mode and FF1 will now set,  $Q_1=1$  and  $Q_1'=0$   
Outputs will change to 0011.

Similarly rest of the operation can be explained.

CLEAR	CLK	$Q_3$	$Q_2$	$Q_1$	$Q_0$	State number	Decimal equivalent
	Initially	0	0	0	0	1	0
1	↓	0	0	0	1	2	1
1	↓	0	0	1	1	3	3
1	↓	0	1	1	1	4	7
1	↓	1	1	1	1	5	15
1	↓	1	1	1	0	6	14
1	↓	1	1	0	0	7	12
1	↓	1	0	0	0	8	8
1	↓	0	0	0	0	1	0

Waveforms of the Johnsons Counter.



EX: The content of a 4 bit shift register is initially 1101. The register is shifted 6 times to right with the serial input being 101101. What is the content of the register AFTER EACH SHIFT. June 07, 8M

CLK	Serial Input	Flip - Flop Output			
		Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
Initially	1	1	1	0	1
1	0	1	1	1	0
2	1	0	1	1	1
3	1	1	0	1	1
4	0	1	1	0	1
5	1	0	1	1	0
6	—	1	0	1	1

Let  $Q_A Q_B Q_C Q_D = 1101$  and apply LSB bit of the number to be entered to  $D_m$ . So  $D_m = Q_A = 1$ .

Apply the 1<sup>st</sup> clock,  $D_m = 1$  the stored word in register is  $Q_A Q_B Q_C Q_D = 1110$

After 2<sup>nd</sup> clock pulse, when  $D_m = 0$  the stored word in register is  $Q_A Q_B Q_C Q_D = 0111$

After 3<sup>rd</sup> clock pulse, when  $D_m = 1$  the stored word in register is  $Q_A Q_B Q_C Q_D = 1011$

After 4<sup>th</sup> clock pulse, when  $D_m = 1$  the stored word in register is  $Q_A Q_B Q_C Q_D = 1101$

After 5<sup>th</sup> clock pulse, when  $D_m = 0$  the stored word in register is  $Q_A Q_B Q_C Q_D = 0110$

After 6<sup>th</sup> clock pulse, when  $D_m = 1$  the stored word in register is  $Q_A Q_B Q_C Q_D = 1011$

## Unit-03/Lecture-11

- The digital circuit used for counting pulses is known as a counter. It is a sequential circuit.

### Asynchronous or Ripple Counters–

For these counters the external clock signal is applied to one FF and then the output of preceding FF is connected to the clock of the next FF.

### Synchronous Counters –

All FF receive the external clock pulse simultaneously. Ring counter and Johnson Counters are examples of Synchronous Counters.

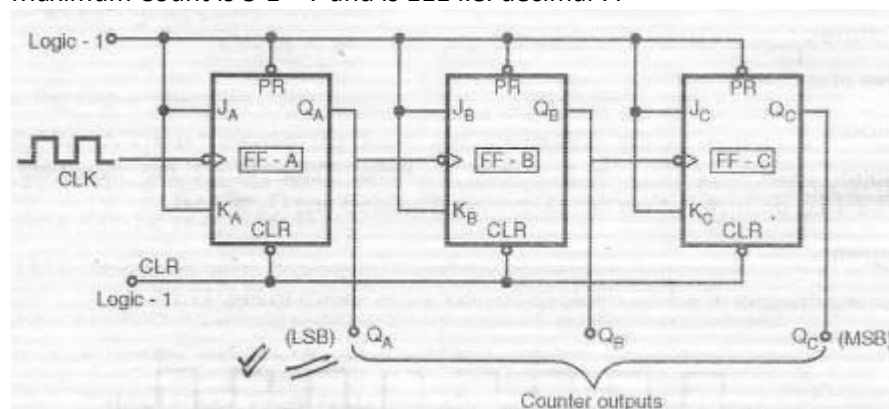
Synchronous and Asynchronous Counters can both be further classified as UP, DOWN or UP/DOWN counters.

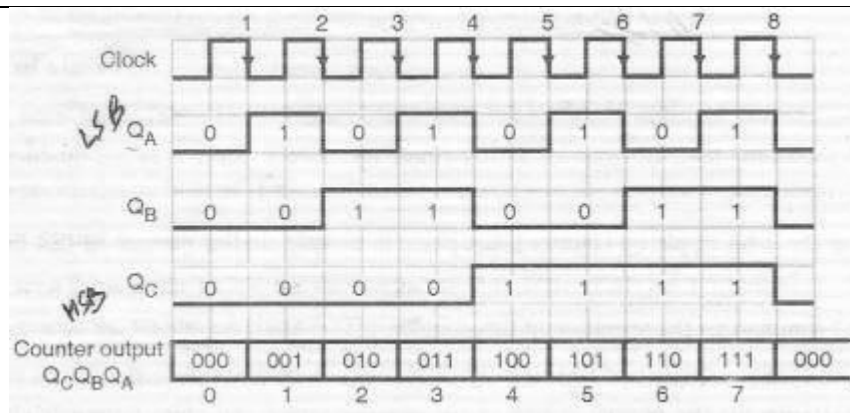
### 3 Bit Asynchronous UP Counter

Clock	Flip-flop outputs			State	Decimal equivalent
	$Q_C$ (MSB)	$Q_B$	$Q_A$ (LSB)		
Initially	0	0	0	1	0
1 <sup>st</sup> (↓)	0	0	1	2	1
2 <sup>nd</sup> (↓)	0	1	0	3	2
3 <sup>rd</sup> (↓)	0	1	1	4	3
4 <sup>th</sup> (↓)	1	0	0	5	4
5 <sup>th</sup> (↓)	1	0	1	6	5
6 <sup>th</sup> (↓)	1	1	0	7	6
7 <sup>th</sup> (↓)	1	1	1	8	7
8 <sup>th</sup> (↓)	0	0	0	1	0

Asynchronous pre-set and clear terminals are also being used. Both of them are active low inputs. Hence for the normal output of the counter pre-set and clear terminals should be connected to 1.

Maximum Count is  $8-1 = 7$  and is 111 i.e. decimal 7.

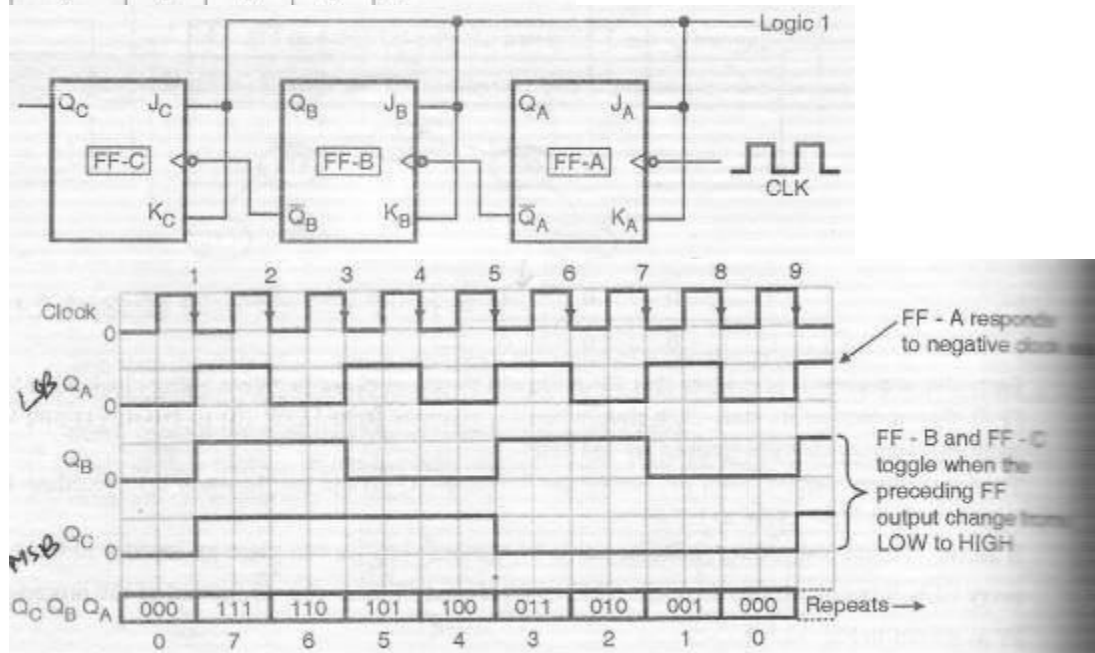




### 3 Bit Asynchronous Down Counter

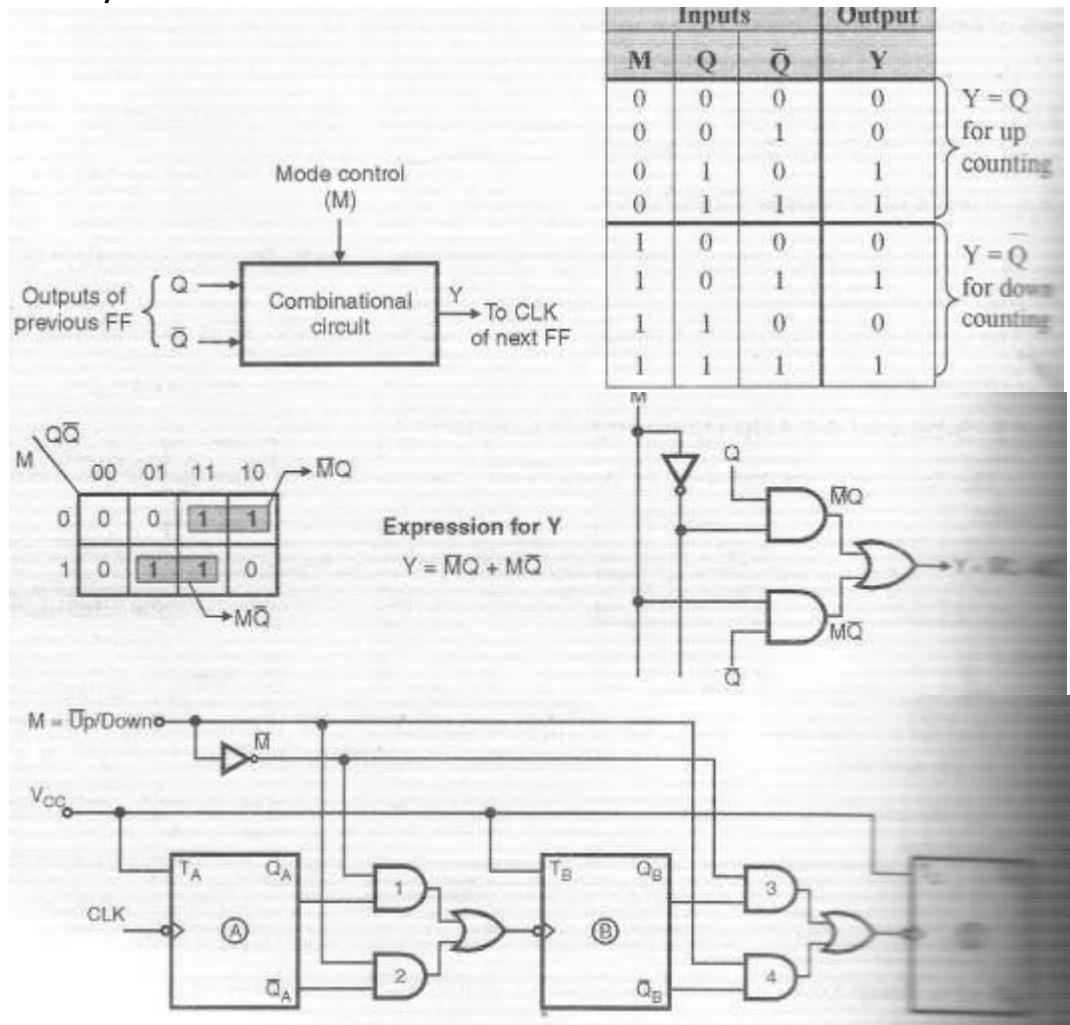
- Counters which count from maximum count to zero are called Down Counters.
- FFA toggles at every edge but FFB changes state each time QA changes from 0 to 1 and QC changes when QB changes from 0 to 1.
- Thus each FF except the FFA toggles when the preceding FF output changes from 0 to 1.

	QC	QB	QA	Flip-flop outputs
7	1	1	1	Recycle
6	1	1	0	
5	1	0	1	
4	1	0	0	
3	0	1	1	
2	0	1	0	
1	0	0	1	
0	0	0	0	





### 3 Bit UP/DOWN COUNTER



#### Applications of the Counters:

- Digital Clock
- Frequency Counting
- Time Measurement
- Digital Voltmeters
- Counter Type A to D Converters
- Digital Triangular Wave Generators
- In Frequency Divider Circuits