UNIT – 4

Digital Logic Families

Unit-04/Lecture-01

Bipolar Families:

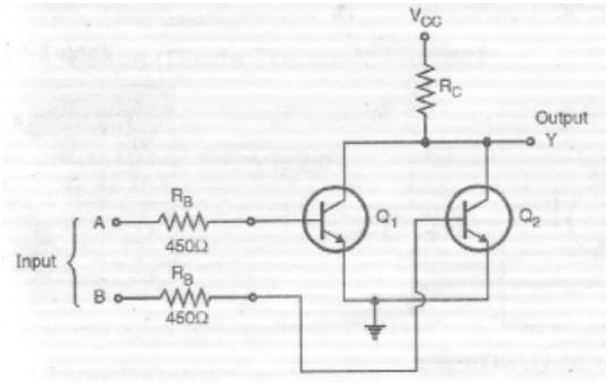
1. Diode Logic (DL)
2. Resistor Transistor Logic (RTL)
3. Diode Transistor Logic (DTL)
4. Transistor- Transistor Logic (TTL)
5. Emitter Coupled Logic (ECL) or Current Mode Logic (CML)
6. Integrated Injection Logic (IIL)

MOS Families:

1. P-MOS Family
2. N-MOS Family
3. Complementary-MOS Family (Consisting of both N MOSand P MOS)

RTL (Resistor Transistor Logic)

- Obsolete now
- It uses resistors and transistors for its implementation



A	B	Q1	Q2	Y (NOR)
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

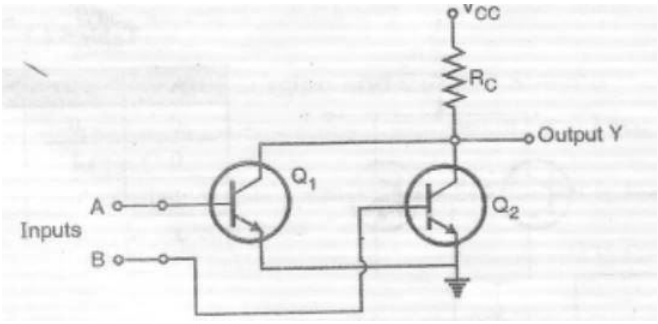
Characteristics of RTL Family

- Poor Noise Margin
- Poor Fan Out
- Low Speed
- High Power Dissipation

Basic Features of RTL

- Popagation delay = 50ns
- Power Dissipation = 10mW
- Noise Margin = 0.2V
- Fan In = 3
- Fan Out = 4
- Relative cost per gate = Medium Value

DCTL (Direct Coupled Transistor Logic)



Disadvantages:

- The reverse saturation current for fan in transistors will get added in Rc, so Y is too low and cannot drive the fan out transistors into saturation.
- Base current of fan out transisitor is almost equal to collector currents and hence will go into deep saturation , hence switching speed is low.
- Output voltage step is low thus reducing noise immunity.
- Transistors are required to have identical characteristics

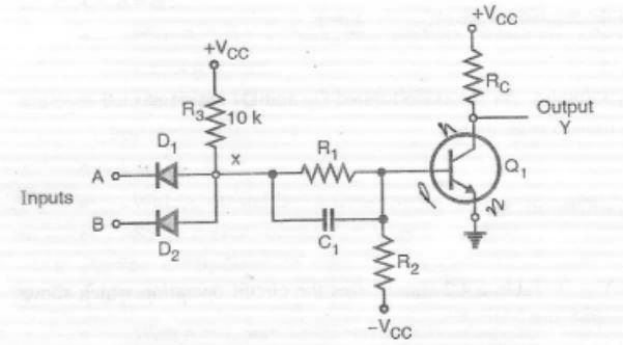
Advantageous:

- A single polarity low voltage supply is required
- Transistors with low breakdown voltages can be used
- Low power dissipation

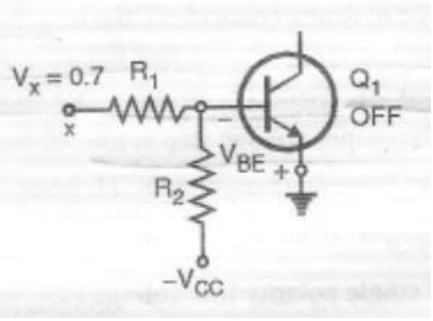
S.NO	RGPV QUESTIONS	Year	Marks
Q.1	Explain the principle of operation of an RTL NOR Gate	Dec 2003	10
Q2	Explain the operation of the RTL NOR Gate	Jun 08	10

Unit-04/Lecture-02

DTL (Diode Transistor Logic)

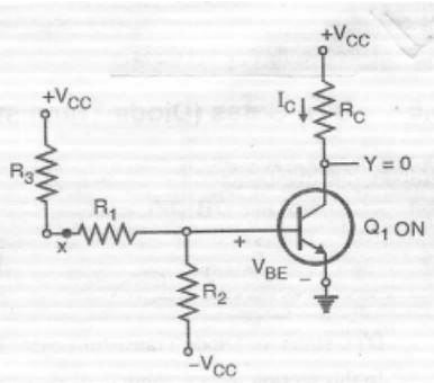


For AB = 00,01,10 the point x will be at 0.7V and equivalent diagram is as shown below



The Y will be HIGH as Q1 is OFF.

For AB = 11 x will be much more than 0.7 so Q1 is switched ON and Y=0. The equivalent diagram is as shown below.



Hence the circuit works as NAND Gate.

Disadvantage of the circuit:

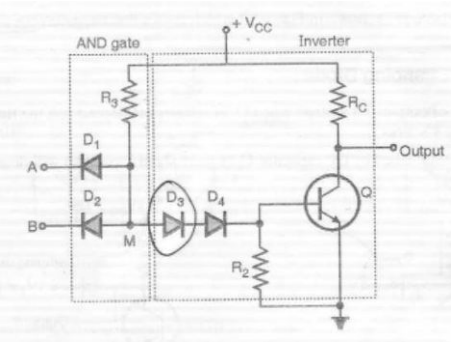
- Capacitor cannot be easily integrated into ICs
- Dual power supply is needed.

S.NO	RGPV QUESTIONS	Year	Marks
Q.1	Explain DTL NAND Gates operation.	Dec. 2007	10

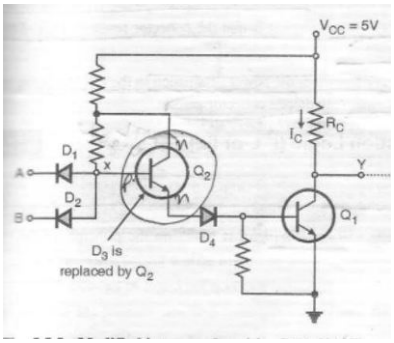
Unit-04/Lecture-03

DTL (Diode Transistor Logic)

Eliminates above disadvantageous. Operation is similar to the one described above.



Fan out can be increased by replacing D3 with Transistor Q2.



Basic Features

- Propagation Delay = 25ns
- Power Dissipation = 15 mW
- Noise Margin = 0.7 V
- Fan In = 8
- Fan Out = 8
- Relative cost per gate = Medium Value

Advantageous:

- Low power Dissipation

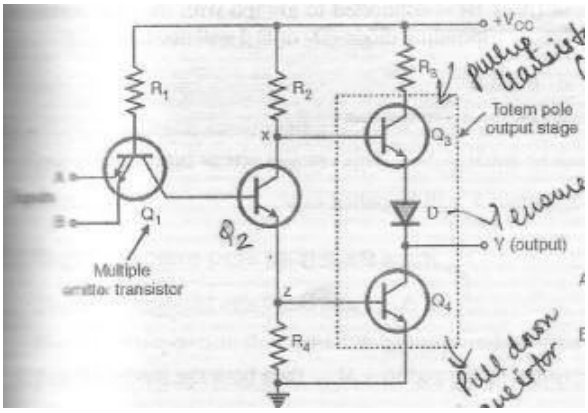
Disadvantageous:

- Poor Noise Margin
- Relatively Low speed

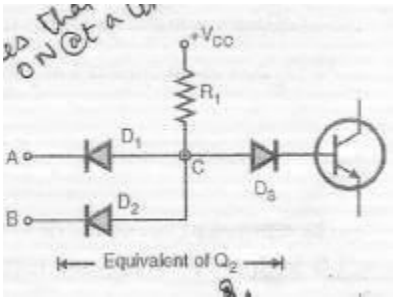
S.NO	RGPV QUESTIONS	Year	Marks
Q.1	Explain DTL NAND Gates operation how the circuit can be changed for increased fan out?	Dec. 2010	10

Unit-04/Lecture-04

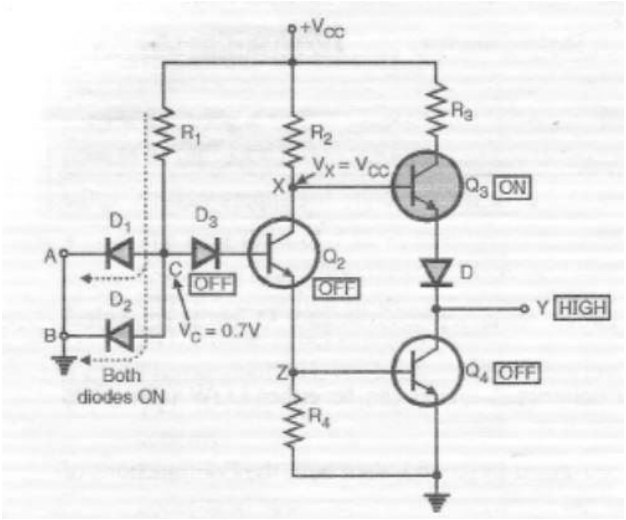
TTL TP (Transistor - Transistor Logic – Totem Pole)



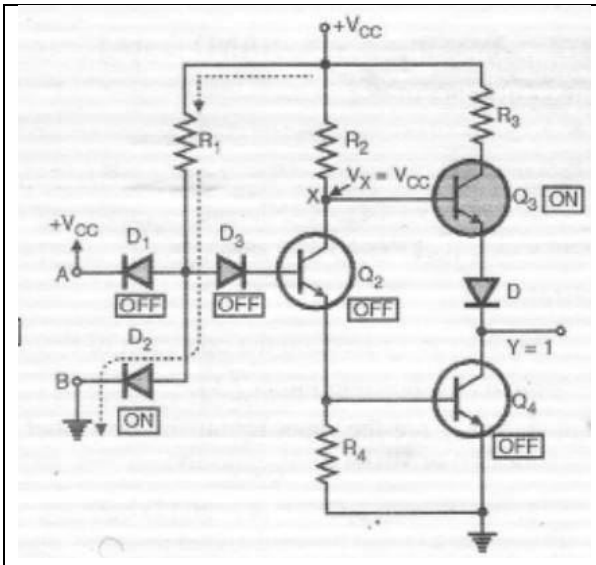
Equivalent Circuit of Totem Pole



When AB = 00 then Vc is at 0.7 V and Transistor Q1, Q2 and Q4 is OFF and Q3 is ON and Y=1.



When AB = 01, 10 then Vc is at 0.7 V and Transistor Q1, Q2 and Q4 is OFF and Q3 is ON and Y=1.



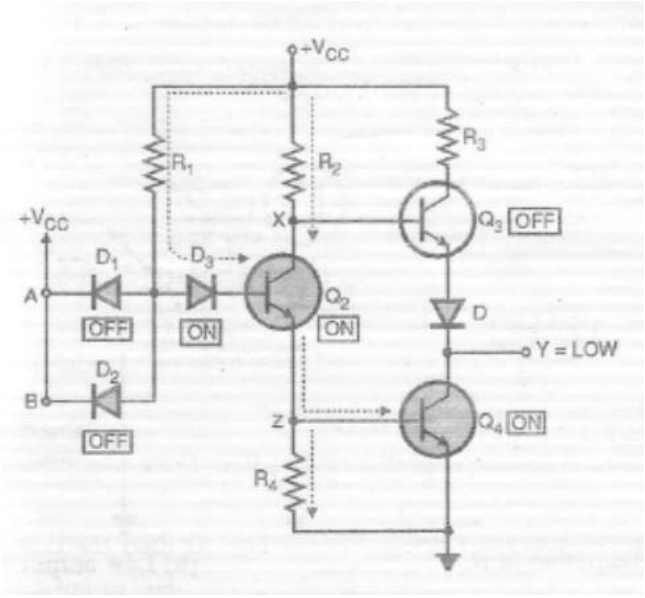
When AB = 11 then Vc is much more than 0.7 V and Transistor Q1, Q2 and Q4 is ON and Q3 is OOF and Y=0. Hence follows NAND operation.

Advantageous of Totem Pole:

- Reduced power dissipation
- Very low output impedance
- Output time constant will be very short for charging up any capacitive load in the output.

Disadvantageous of Totem Pole:

- Q4 turns OFF more slowly than Q3 turns ON. Hence possibility of Both Q3 and Q4 ON simultaneously hence Diode D is used to avoid this condition.



Advantageous of TTL:

- TTL circuits are fast
- Low propagation delay
- Power dissipation is not dependent on frequency

- Compatible to all the other families
- Latch ups do not take place
- These are not susceptible to the damage due to static charges
- Higher current sourcing and sinking capabilities.

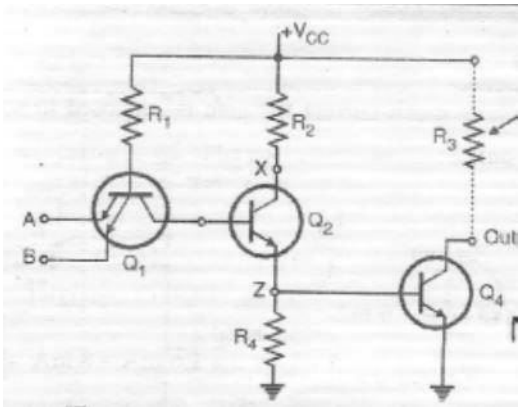
Disadvantageous of TTL:

- Large power dissipation
- Fan out is lower than of CMOS
- Less component density
- Can operate only on +5V power supply
- Poor noise immunity.

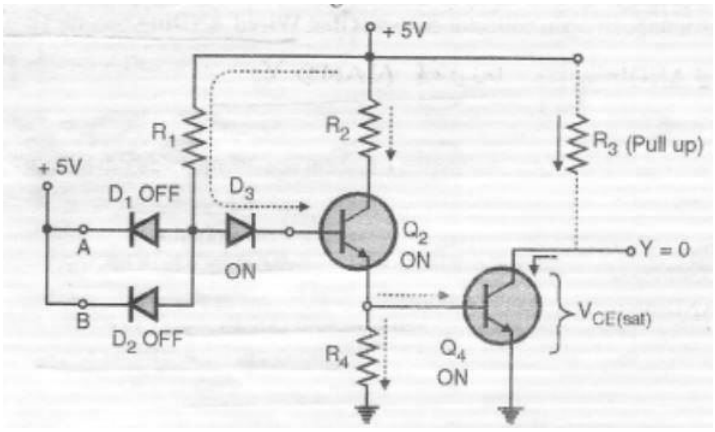
S.NO	RGPV QUESTIONS	Year	Marks
Q.1	Explain TTL in detail with circuit diagram.	Dec. 2005	10
Q.2	Explain the TTL Circuit and verify that it performs NAND operation	Dec 08	10

Unit-04/Lecture-05

TTL-OC (Transistor - Transistor Logic – Open Collector)



Equivalent circuit as shown for AB = 00, 01, 10, Y=1 and AB=11 (as shown) Y = 0. NAND operation.



Disadvantageous:

- R3 is very high, if load capacitance C is large then R3C time constant becomes large and thus slows down the switching speed of he gate.
- Increased power dissipation in R3. This problem is eliminated in Totem Pole arrangement.

Advantageous:

- Wired ANDing is possible.

S.NO	RGPV QUESTIONS	Year	Marks
Q.1	Write short notes on Open Collector TTL	Jun. 2007	7

Unit-04/Lecture-06

TTL – Tristate Logic

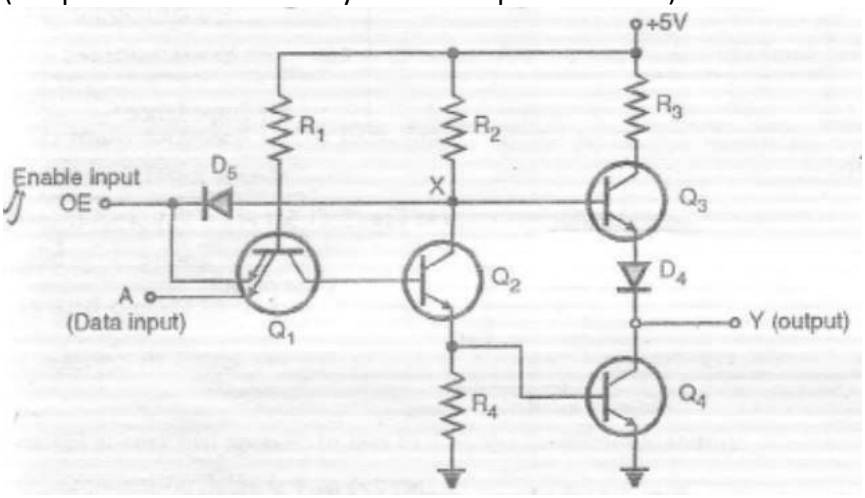
Three possible states:

1. HIGH
2. LOW
3. HIGH IMPEDENCE OR HIGH-Z State

Additional OE is introduced.

When OE=1 the circuit operates as inverter. A=0 then Y=1 or vice-versa.

When OE=0 then irrespective of the input Q3 and Q4 will be OFF thus achieving HIGH-Z state (Output not connected anywhere or open circuited).



Summary of Operation

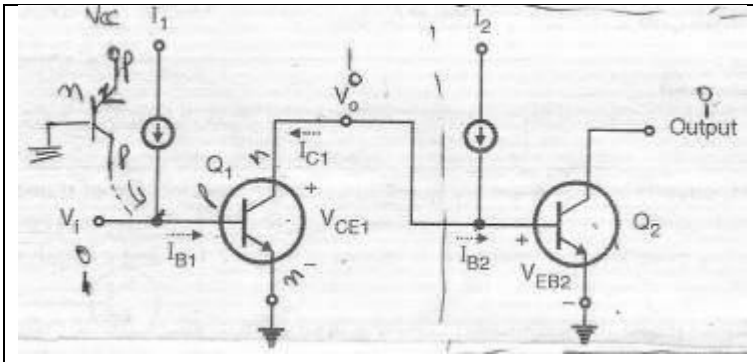
OE	A	Y	State
0	X	Floats	High Impedence
1	0	0	Low
1	1	1	High

Advantageous:

- Outputs of Transistors are connected together they can share a common wire.
- We get all the advantageous of totem pole such as low output impedance and high speed.

IIL – Integrated Injection Logic

The 2nd current source and Q2 functions as a basic not gate. Q2 becomes saturated early as additional current is supplied by active load (Here current source)



1. Vi = 0, Q1 OFF IB1 = 0 Input source acts like a sink for I1. I2 flows through Q2 and drives it in saturation. Q2=ON output Y = 0.
2. Vi=1, Q1 =ON (Saturation) VCE1= 0.3 Q2 =OFF. Q1 acts as sink for I2. Y=1.

Features:

- Propagation delay = 40ns
- Power dissipation: <1mW (because of active load)
- Poor noise margin = 0.35V
- Fan in = x
- Fan out: 8 (Multiple Collector Terminals)
- Relative Cost : very low

Advantages:

- Speed-power product is constant and has relatively low value
- Very high packing density
- Low cost

Disadvantages:

- Low speed
- Poor Noise Margin

Characteristics

- Speed of operation depends on the charging current
- Propagation delay is inversely proportional to charging current
- Power dissipation is proportional to charging current
- Figure of Merit is in the range of 0.1 to 0.1 PJ
- Very small silicon area is required
- Packaging density is in the range of 120 to 200 gates per sq mm.

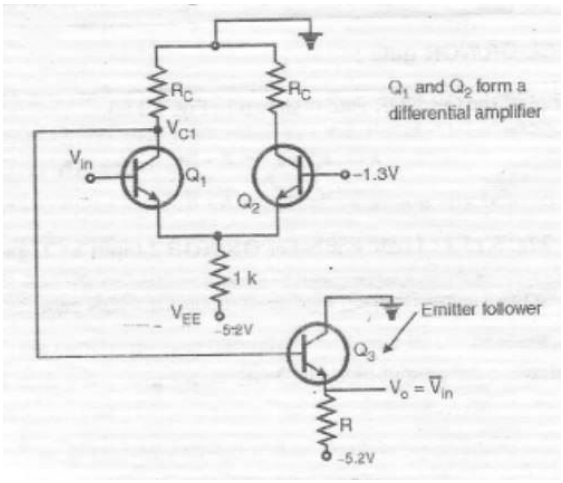
S.NO	RGPV QUESTIONS	Year	Marks
Q.1	Explain Tristate TTL operation	Jun. 2005	7
Q2	Explain the Functioning of I^2L Logic with the help of circuit	Dec 2014	10

Unit-04/Lecture-07

ECL (Emitter Coupled Logic)

Transistors in ECL do not go into saturation (either operate in active or cut off region) hence it is possible for them to switch at faster speeds as compared to TTL logic.

ECL NOT Gate

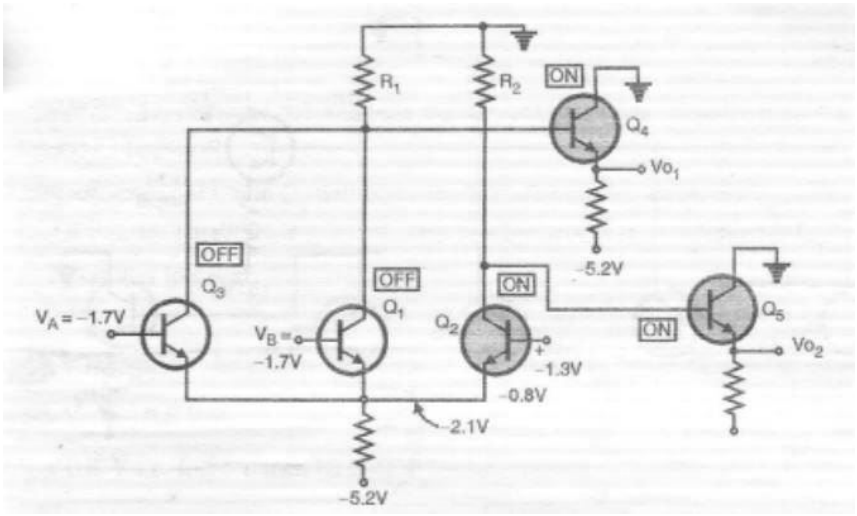


Operation Summary:

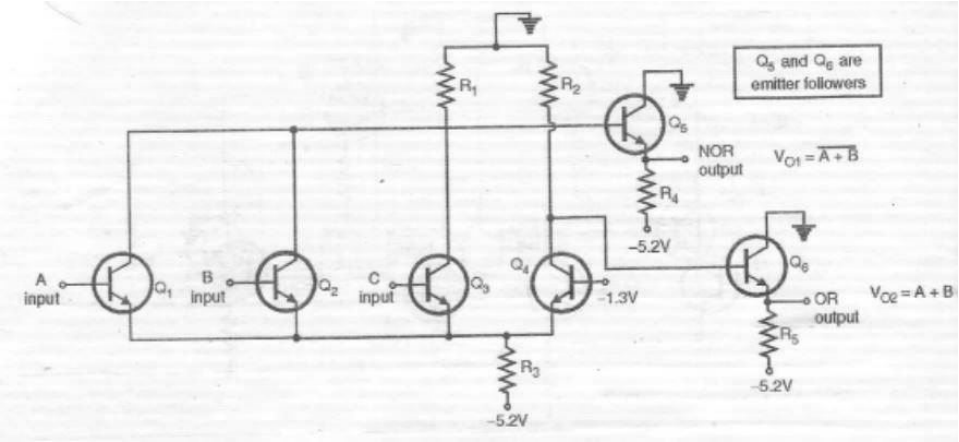
Vin	Q1	Q2	Vc1	Vc2	Vo = Vc1-0.8
-1.7 (logic 0)	OFF	ON	0	-0.9	-0.8 (Logic 1)
- 0.8 (Logic 1)	ON	OFF	-0.9	0	-1.7 (Logic 0)

ECL 2 input OR/NOR Gate

When AB = 00 voltages are as shown below.Q1 and Q3 = OFF and Q2, Q4 and Q5 = ON Thus V01 = HIGH and is NOR output. And V02 = LOW and gives OR output.



Example: 3 Input ECL OR/NOR Gate



Operation is similar to the one mentioned above.

Advantageous:

- It is fastest of logic family
- High fan out due to high input resistance and low output resistance
- Excellent speed power product
- It can provide two outputs simultaneously i.e. OR and NOR, no additional inverter is needed

Disadvantageous:

- High power dissipation
- Its high speed generates VI transients
- Limited logic swing hence vulnerable to noise.

Basic Features:

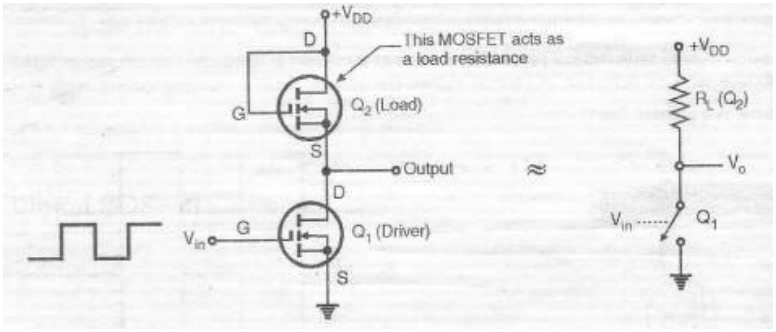
- Propagation Delay : 2ns
- Power Dissipation: 50mW
- Noise Margin 0.4V
- Fan In: 5
- Fan Out: 25
- Relative Cost : High

S.NO	RGPV QUESTIONS	Year	Marks
Q.1	Why the speed of operation of ECL is highest among all saturated and non saturated logic families?	Dec 2006	5
Q.2.	Write short notes on ECL logic family	Jun 07	7
Q.3.	Write short note on ECL family	Dec 10	5

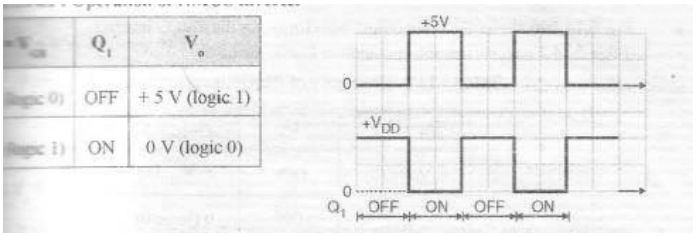
Unit-04/Lecture-08

PMOS uses P and NMOS used N, channel enhancement MOSFETs (Metal Oxide Semiconductor Field Effect Transistors)

NMOS

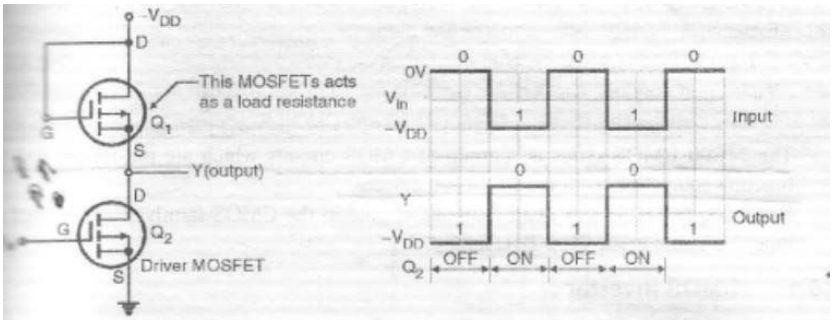


Q1 acts as switch ON when Vin= HIGH and vice versa.



	Q_1	V_o
(logic 0)	OFF	+ 5 V (logic 1)
(logic 1)	ON	0 V (logic 0)

PMOS



When Vin=0 then Y=HIGH and when Vin=-5V then Y=0.

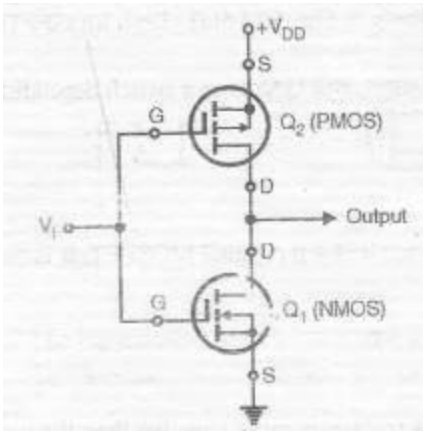
Input V_{in}	Q_2	Output Y
0 Volts (0)	OFF	$-V_{DD}$ (1)
$-V_{DD}$ (1)	ON	0 (logic 0)

S.NO	RGPV QUESTIONS	Year	Marks
Q.1	Write a short note on NMOS and PMOS logic gates	Dec 2007	5

Unit-04/Lecture-08

CMOS

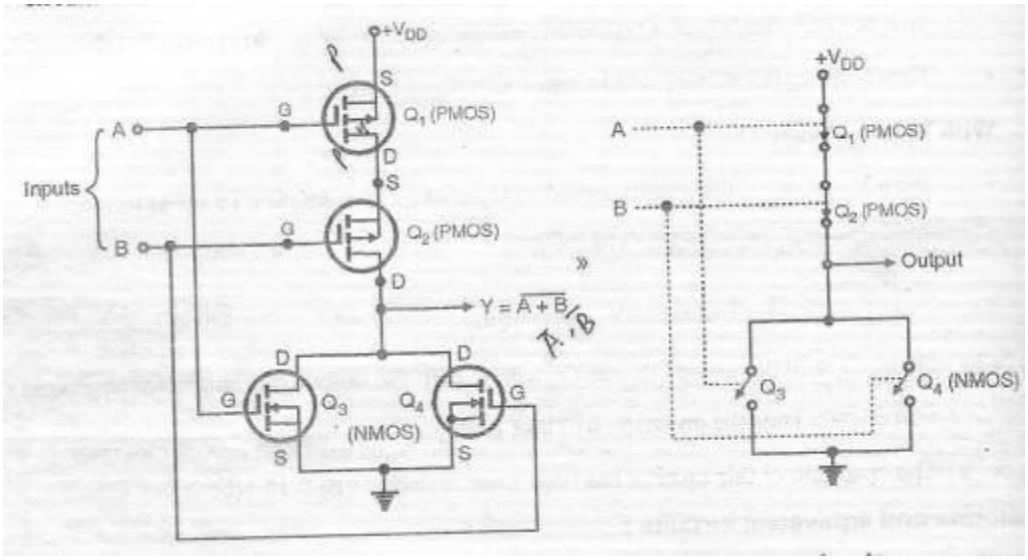
CMOS uses both P and N Channel MOSFETs



V_i	Q_1	Q_2	Output
0V (logic 0)	OFF	ON	V_{DD} (logic
V_{DD} (logic 1)	ON	OFF	0 (logic 0

When Vi=0 then Q1=OFF, V_{GS} of Q2 = $-V_{DD}$ Q2=ON, hence Y=1
When Vi=1 then Q1=ON , Q2 = OFF hence Y=0

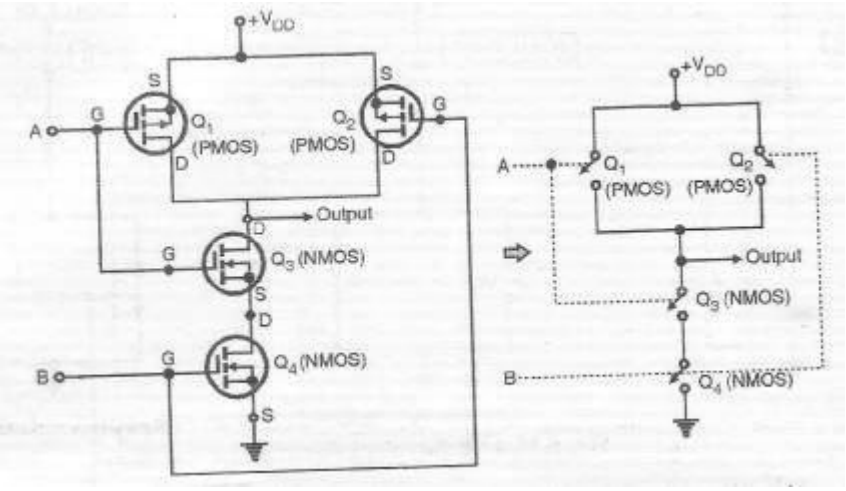
CMOS NOR



Operation Summary:

Input	Input	Transistor	Transistor	Transistor	Transistor	Output
A	B	Q1	Q2	Q3	Q4	Y
0	0	ON	ON	OFF	OFF	Vdd = 1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

CMOS NAND



Operation Summary:

Input	Input	Transistor	Transistor	Transistor	Transistor	Output
A	B	Q1	Q2	Q3	Q4	Y
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Advantageous:

- Low power dissipation
- High fan out
- High noise margin for higher values of V_{DD}
- Capable of working over a wide range of supply voltage
- Switching speeds comparable to those of TTL
- High packaging density since MOS devices need less space

Disadvantageous:

- Propagation delays longer than those of TTL
- Slower than TTL
- Susceptible to damages due to static charge
- Latch ups can take place
- Need protection circuitry.

S.NO	RGPV QUESTIONS	Year	Marks
Q.1	Explain CMOS logic with its merits and demerits	Jun 2004	10
Q.2	Distinguish between NMOS, PMOS and CMOS	Dec 2006	10