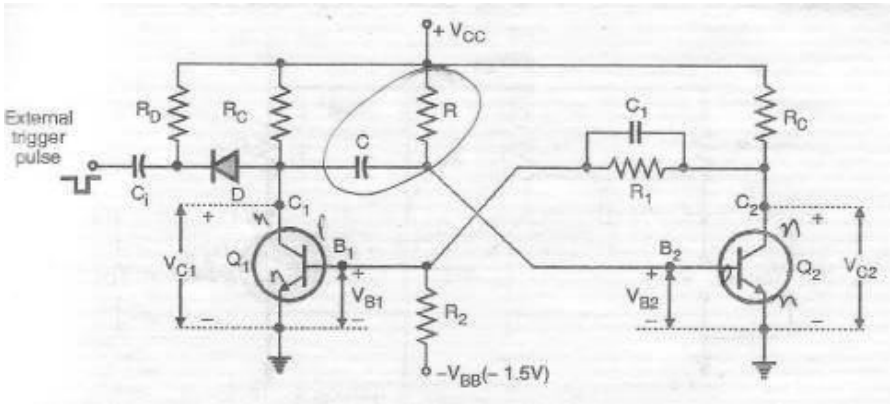
UNIT – 5

Clocks and Timing Circuits

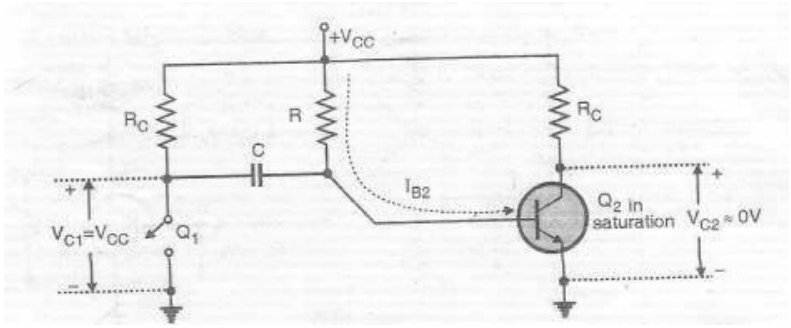
Unit-05/Lecture-01

Monostable Multivibrator

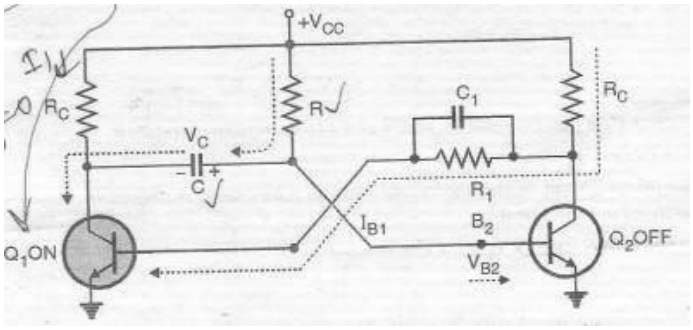
- 1 stable, 1 quasi stable state



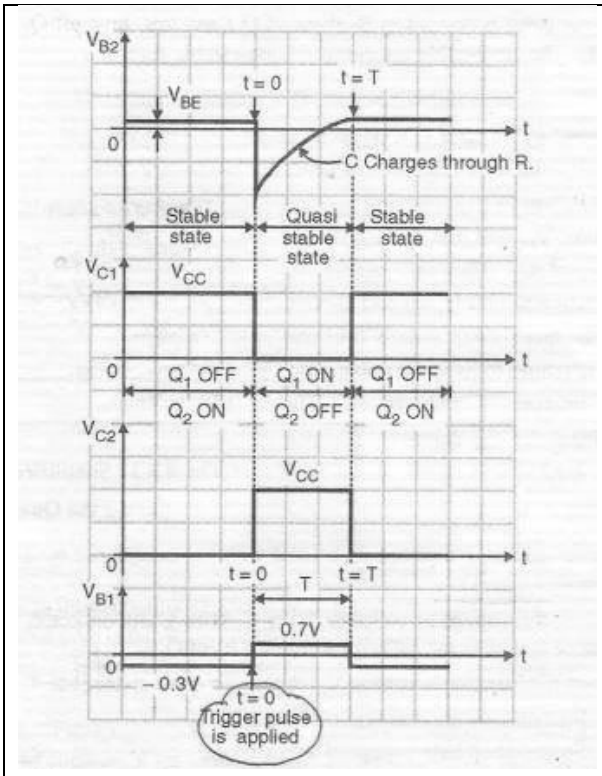
The equivalent diagram in the initial state (Stable State) is as below



The equivalent diagram in the quasi stable state is as below



The waveforms of monstablemultivibrator is as shown.



$$V_\gamma = V_{CC} - (V_{CC} - V_\sigma + I_1 R_C)\, e^{-T/\tau}$$

$$\therefore e^{-T/\tau} = \frac{V_{CC} - V_\gamma}{(V_{CC} - V_\sigma + I_1 R_C)} \approx \frac{V_{CC} - V_\sigma + I_1 R_C}{V_{CC} - V_\gamma} = e^{T/\tau}$$

$$\therefore \frac{T}{\tau} = \log_e \left[\frac{V_{CC} - V_\sigma + I_1 R_C}{V_{CC} - V_\gamma} \right]$$

$$\therefore T = \tau \log_e \left[\frac{V_{CC} - V_\sigma + I_1 R_C}{V_{CC} - V_\gamma} \right]$$

Derivation for the expression for Time Period T is as below.

$$T = \tau \log_e \left[\frac{2V_{CC} - V_{CE(sat)} - V_{BE(sat)}}{V_{CC} - V_\gamma} \right] = \tau \log_e 2 + \tau \log_e \left[\frac{V_{CC} - V_{CE(sat)} - V_{BE(sat)}}{2} \right]$$

At room temperature,

$$V_{CE(sat)} + V_{BE(sat)} \approx 2V_\gamma \quad \ldots$$

Substituting, we get

$$T = \tau \log_e 2 + \tau \log_e \left[\frac{V_{CC} - V_\gamma}{V_{CC} - V_\gamma} \right] = \tau \log_e 2$$

But $\log_e 2 = 0.69$

$$\therefore T = 0.69\,\tau = 0.69\,(R_0 + R)\,C \quad \ldots$$

But in saturation, $R_0 \ll R$

$$\therefore T \approx 0.69\,RC \quad \ldots$$

Applications:

- As Timer and delay generator

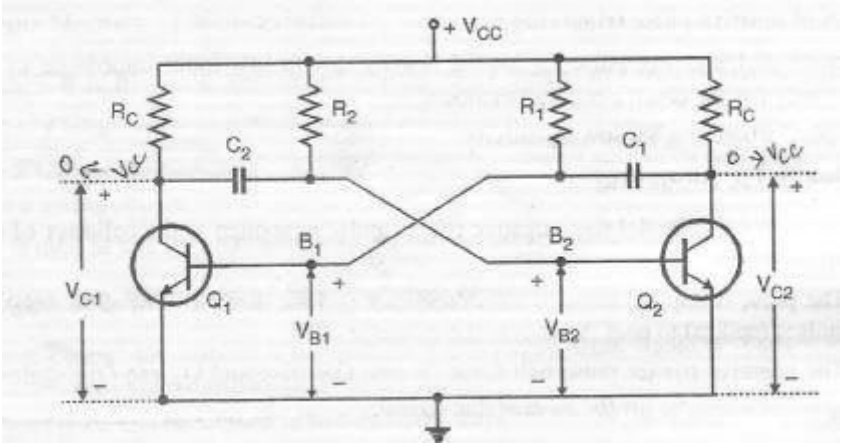
UNIT – 5

Clocks and Timing Circuits

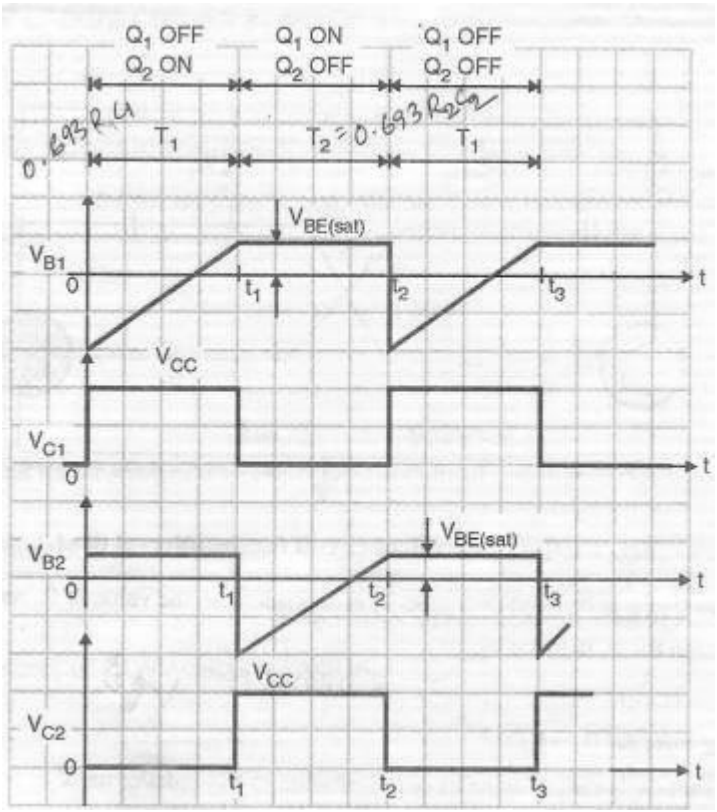
Unit-05/Lecture-02

AstableMultivibrator

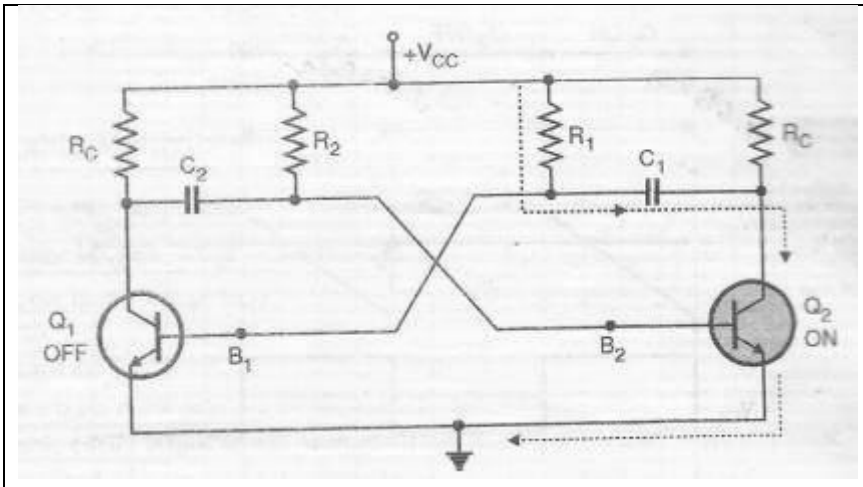
- Both states are quasi stable or it has no stable state and hence always changing its state



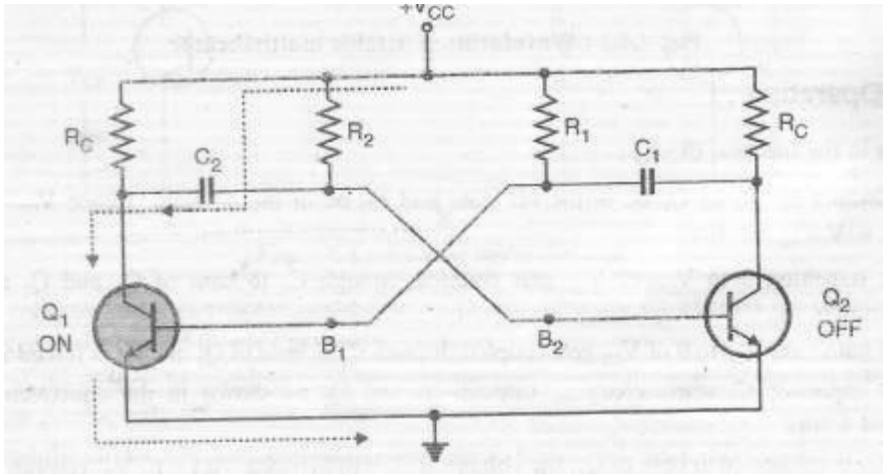
Waveforms of astablemultivibrator



Equivalent circuit for the interval 0-t_1



Equivalent circuit for interval t_1-t_2



Design equations of astablemultivibrator

$T_1 = 0.69\ R_1\ C_1$

$T_2 = 0.69\ R_2\ C_2$

$T = T_1 + T_2 = 0.69\ (R_1\ C_1 + R_2\ C_2)$

$f = 1/T$

$$\text{Duty cycle } D = \frac{T_2}{T_1 + T_2} = \frac{R_2\ C_2}{R_1 C_1 + R_2\ C_2}$$

$$I_C \approx \frac{V_{CC}}{R_C} \quad \text{.... assuming } V_{CE(sat)} = 0$$

$$I_B = \frac{V_{CC}}{R_1} = \frac{V_{CC}}{R_2} \quad \text{....assuming } V_{BE(sat)} = 0$$

Applications:

- Rectangular wave generator
- Square wave generator
- Flasher Circuit
- Ramp Generator

Timing and Duty Cycle considerations for AstableMultivibrator.

$$T = 0.69\,RC$$

Similarly we can prove that

$$T_1 = 0.69\,R_1\,C_1$$

$$\text{And } T_2 = 0.69\,R_2\,C_2$$

So the total time corresponding one complete cycle of output is given by

$$T = T_1 + T_2 = 0.69\,(R_1\,C_1 + R_2\,C_2)$$

For a symmetrical astable circuit,

$$R_1 = R_2 = R \text{ and } C_1 = C_2 = C$$

$$\therefore T = 0.69\,(RC + RC) = 1.38\,RC$$

The frequency of astable output is given by,

$$f = \frac{1}{T} = \frac{1}{1.38\,RC} = \frac{0.7246}{RC}$$

It is possible to vary the frequency by adjusting the values of R and C. But it change T and f by connecting R_1 and R_2 to an auxiliary supply voltage of – V.

Then the expression for time period is given by,

$$T = 2RC \log_e\left[1 + \frac{V_{CC}}{V}\right]$$

For proper operation of this circuit, the following condition should be satisfied

$$V > 0.7 \text{ or } 0.3\,V$$

Such on astable circuit is called as a voltage to frequency converter.

5 Duty Cycle :

Duty cycle is defined as the ratio of on time to the total time.

If we assume that the output is obtained at the collector of Q_2, then the duty cy

$$D = \frac{T_2}{T_1 + T_2} = \frac{0.69\,R_2\,C_2}{0.69\,(R_1C_1 + R_2C_2)}$$

$$= \frac{R_2\,C_2}{R_1C_1 + R_2\,C_2}$$

Duty cycle varies between 0 and 1. It can also be expressed as a percentage as

$$\%\,D = \frac{R_2\,C_2}{R_1C_1 + R_2\,C_2} \times 100$$

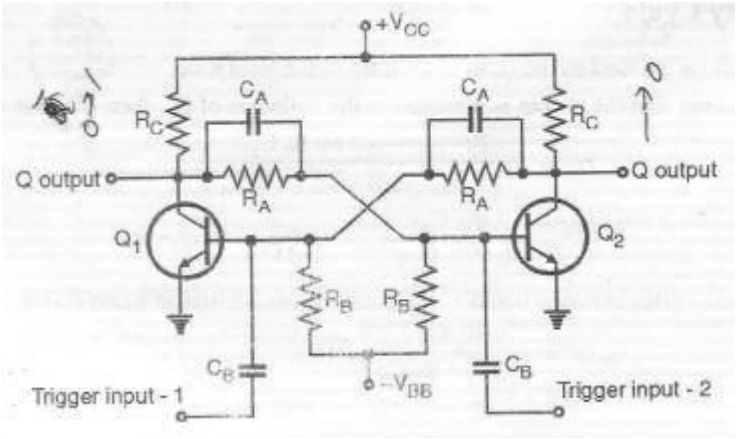
UNIT – 5

Clocks and Timing Circuits

Unit-05/Lecture-03

BistableMultivibrator

- It has 2 possible states of operation (Both Stable)
- Once the multivibrator enters in one stable state, it continues to be in that state, until it is forced to change the state by an external excitation.



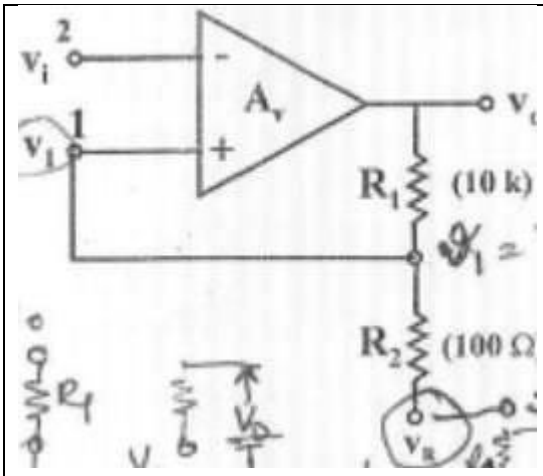
Q1	Q2	Q output	Q' output
ON	OFF	HIGH	LOW
OFF	ON	LOW	HIGH

Applications:

- Flip Flop
- Memory cell to store 1 bit information
- Basic unit to build registers and counters.

Schmitt Trigger (Regenerative Comparator)

- It is modified version of bistablemultivibrator



Assuming vi < V1 so that v0 = +5V then using superposition

$$v_1 = \frac{R_1 V_R}{R_1 + R_2} + \frac{R_2 V_o}{R_1 + R_2} = V_1$$

If v1 is now increased then v0 remains constant at v0 and vi = V1 = constant until vi = V1. A this threshold, critical or triggering voltage, the output regeneratively switches to V0 = -V0 and remains at this value as long as vi > V1

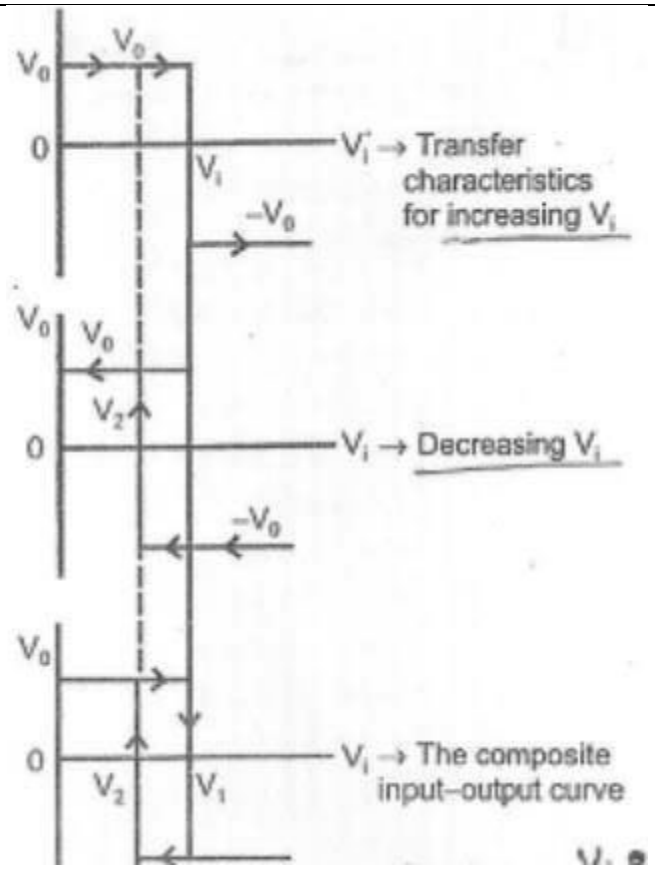
The voltage at the non inverting terminal is

$v_1 > V_1$ is

$$v_1 = \frac{R_1 V_R}{R_1 + R_2} - \frac{R_2 V_o}{R_1 + R_2} = V_2$$

$$\text{Hysteresis } V_H = V_1 - V_2 = \frac{2 R_2 V_o}{R_1 + R_2}$$

The Waveforms are as shown below



Applications of Schmitt Trigger

- The most importing use is to convert a very slowly varying input voltage into an output having an abrupt wave form occurring at a precise value of input voltage.
- Comparator
- Squaring Circuit

UNIT – 5

Clocks and Timing Circuits

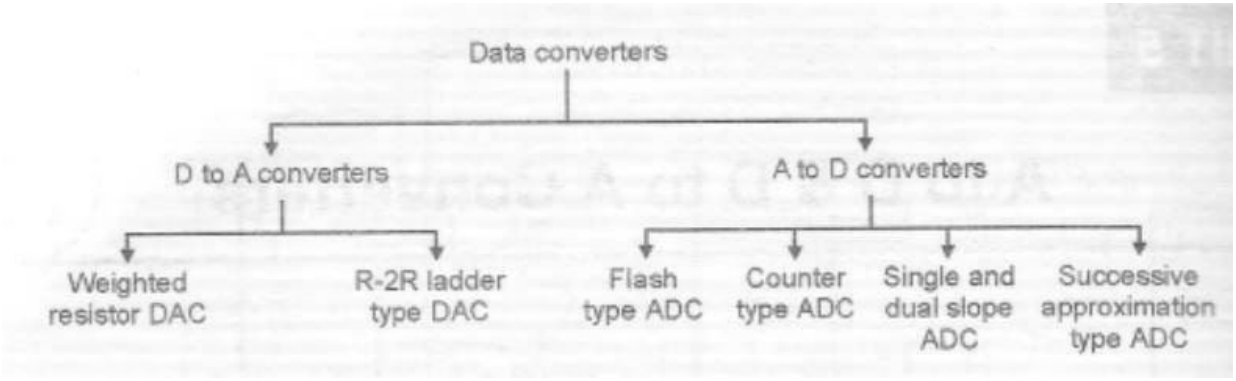
Unit-05/Lecture-04

Quantities like temperature, pressure, displacement, vibrations are analog signals but difficult to measure hence there is a need to convert them to digital for ease of processing, storing and transmitting.

Types:

D to A Digital to Analog conversion

A to D Analog to Digital conversion

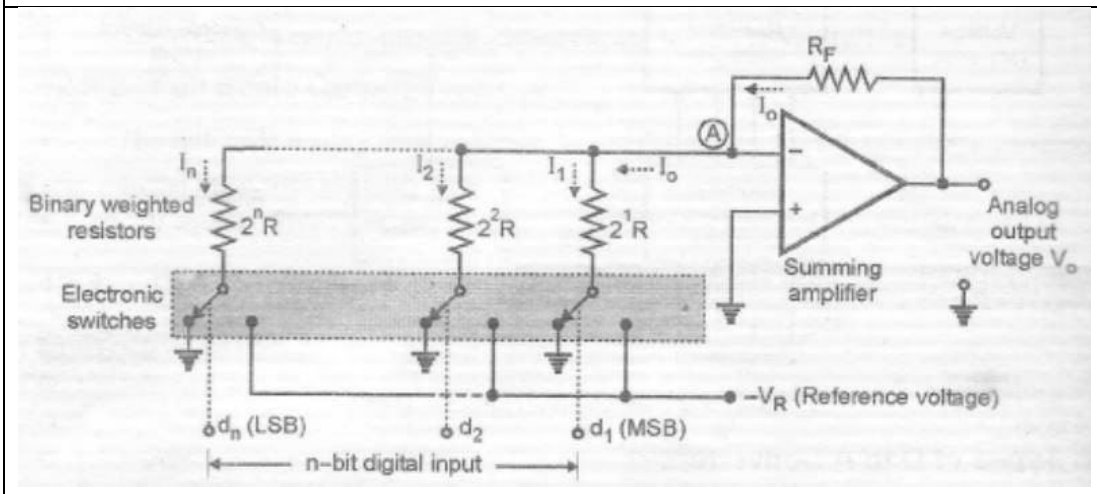


Specifications for DAC

- Resolution – smallest possible change in output voltage and depends on bits applied at the input
- Accuracy – Closeness of the output voltage to theoretical value
- Linearity – input and Output should be linear (may not be so due to errors)
- Temperature Sensitivity - Changes to the output due to temperature variation
- Settling time – The time required to settle the analog output within ½ of LSB of the final value, after the change in digital input is called settling time. It should be as short as possible.
- Speed – Time needed to perform a conversion from digital to analog or vice versa. Conversions performed per second
- Long Term Drift – Mainly due to resistor and semiconductor aging effecting linearity, speed etc.
- Supply Rejection – It Indicates the ability of DAC to maintain scale, linearity etc. when the supply voltage is varied.

Unit-05/Lecture-05

Binary Weighted Resistor DAC (n bit DAC)



$$I_o = I_1 + I_2 + \ldots + I_n = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2R} d_2 + \ldots + \frac{V_R}{2^nR} d_n$$

d_n can have a value of either "0" or "1".

$$\therefore \quad I_o = \frac{V_R}{R} \left[d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n} \right]$$

V_o is given by,

$$V_o = I_o R_F = V_R \cdot \frac{R_F}{R} \left[d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n} \right]$$

expression for output voltage.

ations (12.5.2) and (12.5.3), we can conclude that,

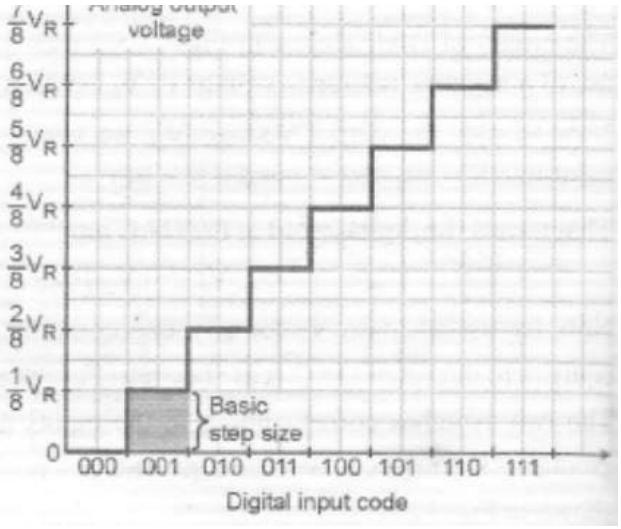
$$K = \frac{R_F}{R} \text{ and } V_{FS} = V_R.$$

= 1.

$$V_o = V_R \left[d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n} \right]$$

Example : 3 bit Weighted resistor DAC

Digital input			Analog output
d_1	d_2	d_3	Voltage V_o
0	0	0	0
0	0	1	$V_R/8$
0	1	0	$2V_R/8$
0	1	1	$3V_R/8$
1	0	0	$4V_R/8$
1	0	1	$5V_R/8$
1	1	0	$6V_R/8$
1	1	1	$7V_R/8$



Advantageous:

- Simple circuitry
- Easy Calculations

Disadvantageous:

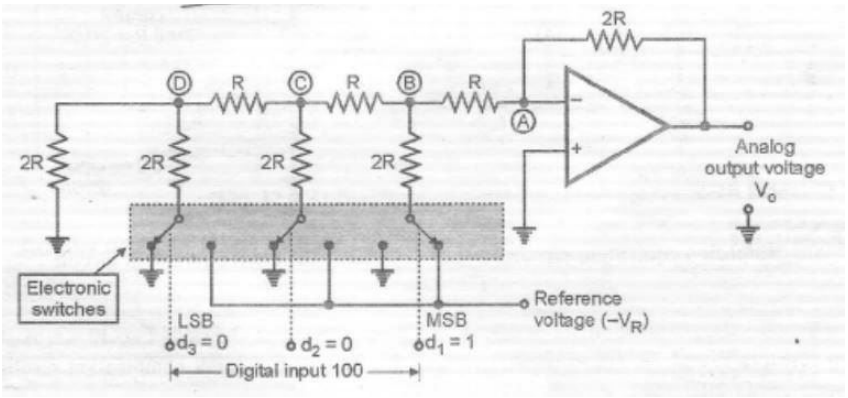
- The accuracy and stability depends on the resistors used.
- It requires wide range of resistor values
- The smallest resistance cannot be smaller than 2.5KOhm to avoid loading effect
- To maintain accurate ration over wide range of resistors values restricts it for values less than 8 bits therefore resolution of such a DAC is poor.
- The finite resistance of the switches will disturb the currents particularly in MSB where the current setting resistors are small in value.

Sources of Error in DACs

- Linearity Error – The amount by which the actual output differs from ideal straight line transfer characteristics.
- Offset Error – It is the nonzero level of analog output when all the digital inputs are 0. The offset is due to the offset voltages of OP-AMPS and leakage currents in the switches.
- Gain Error – It is the difference between the calculated gain and practically obtained gain. The error exists due to the error in the feedback resistor value.

Unit-05/Lecture-06

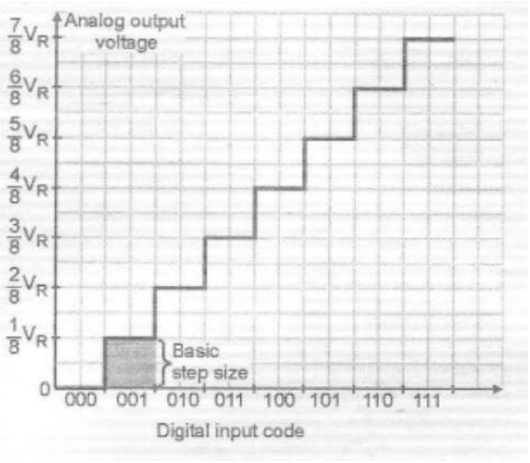
R-2R Ladder



Operation

Let input =100, R = 2.5 KOhm to 10KOhm. Point A is virtual ground. Applying Thevenins theorem at point A to calculate the equivalent resistance (R_{eq}) and then calculating the $Vo = -(2R/R_{eq})V_R$

Digital input			Analog output voltage V_o
d_1	d_2	d_3	
0	0	0	0
0	0	1	$V_R/8$
0	1	0	$2V_R/8$
0	1	1	$3V_R/8$
1	0	0	$4V_R/8$
1	0	1	$5V_R/8$
1	1	0	$6V_R/8$
1	1	1	$7V_R/8$



Advantageous:

- It is easy to build this circuit accurately
- Increase in bits are possible by adding R/2R values
- The current flowing away from the nodes is equal to current flowing towards the right of the circuit.
- It can be fabricated monolithically, accurately and with stability due to small resistance spread.

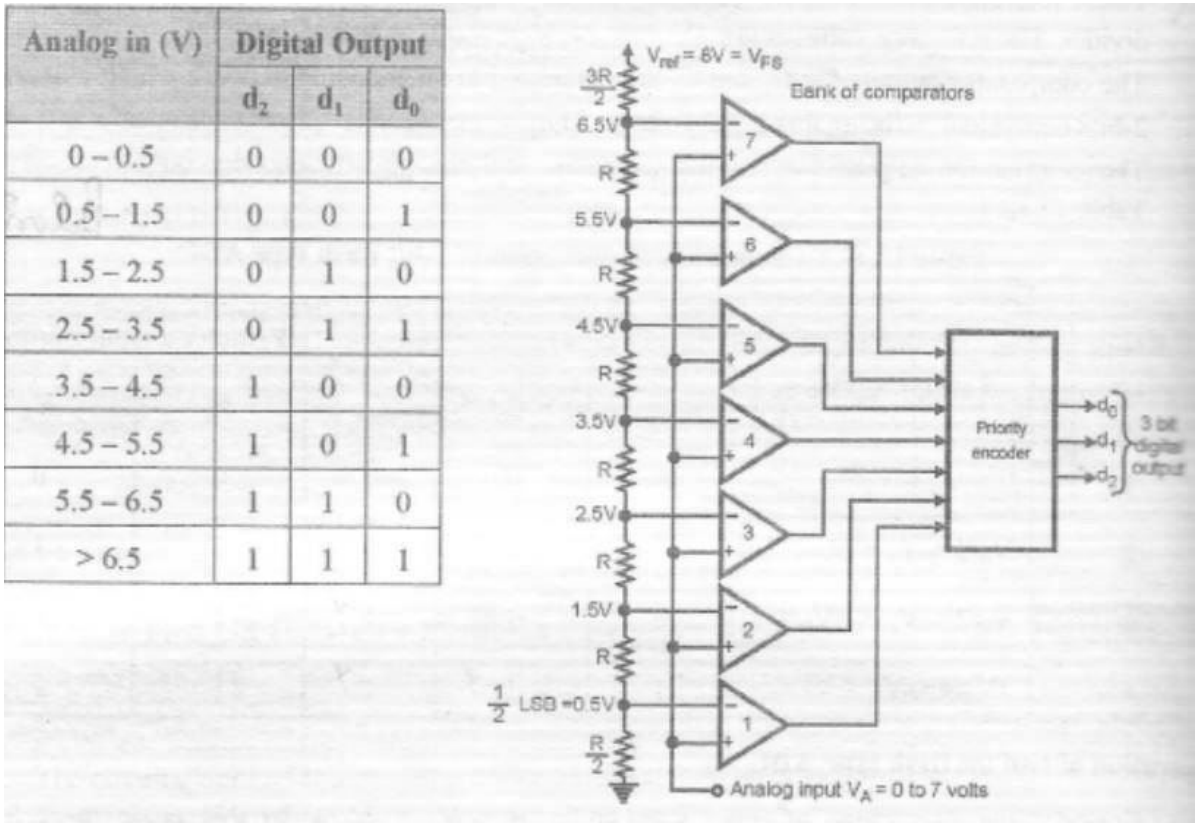
Applications:

- Motion speed Control
- Counter ADC and Successive approximation ADC
- CRT or XY Plotter
- Computers and Electronic Equipment's like curve tracers

UNIT – 5/ Lecture 7

3 Bit Flash Type ADC

Analog in (V)	Digital Output		
	d_2	d_1	d_0
0 – 0.5	0	0	0
0.5 – 1.5	0	0	1
1.5 – 2.5	0	1	0
2.5 – 3.5	0	1	1
3.5 – 4.5	1	0	0
4.5 – 5.5	1	0	1
5.5 – 6.5	1	1	0
> 6.5	1	1	1



Operation:

- The resistance ladder is used to generate different reference voltages from 0.5 to 6.5V
- The reference voltages are applied to Comparators. The analog input V_A is applied to non-inverting terminals of all the comparators.
- The comparator outputs are applied to a priority encoder which produces a 3 bit digital output.

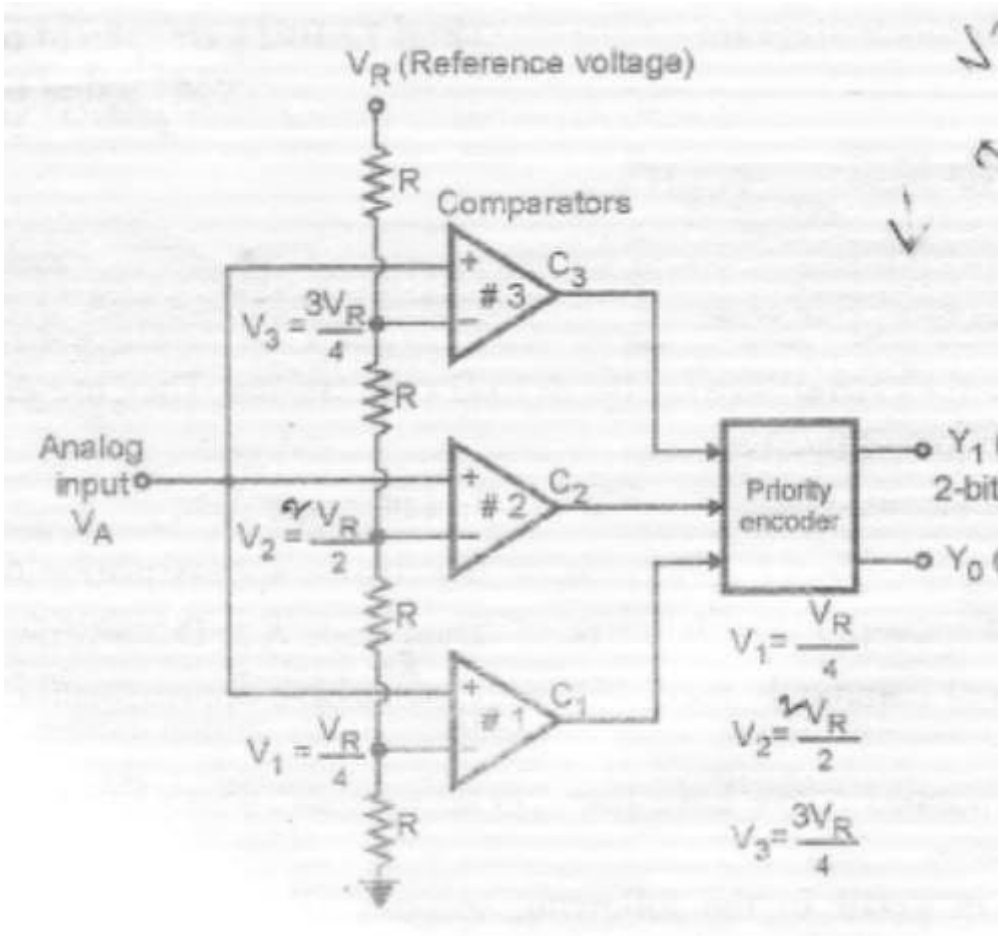
Advantageous:

- High speed of conversion due to parallel operation
- Typically speed is less than 100ns

Disadvantageous:

- Large numbers of comparators are required. With increase in the number of bits by 1, the number of comparators will approximately double.
- Encoder complexity increases with increase in the number of bits.

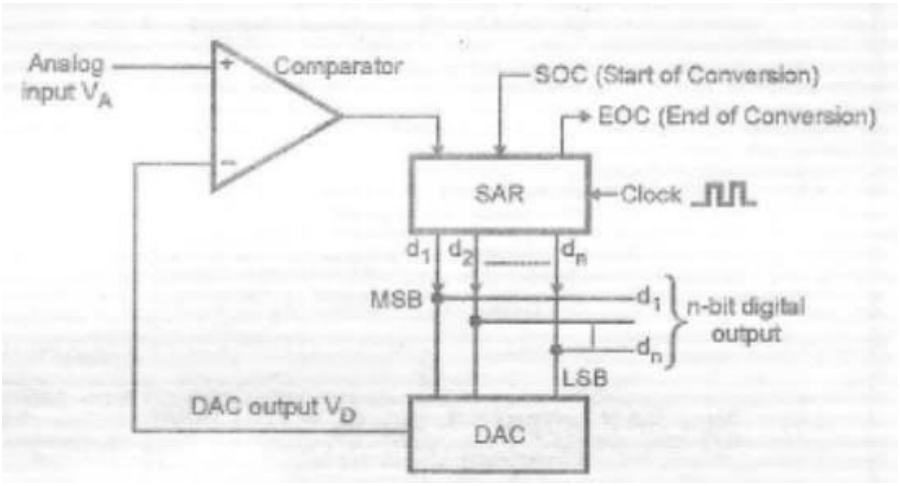
Example : 3 Bit Flash type ADC



UNIT – 5/ Lecture 8

Successive Approximation ADC (SA-ADC)

n = variable and T = Time period of clock



- Conversion is started by SOC line.
- The SAR 1st tries HIGH on MSB (SAR outputs half of its full scale output) and the result is compared by comparator, if its output is higherthan V_A, the SAR returns the MSB LOW. If the DAC output was still lower than the unknown analog input voltage, the SAR leaves the MSB HIGH.
- The Lower bit is tried and the same procedure is repeated
- After the end when all the bits are tested (LSB is reached) the SAR output is the equivalent unkownanalog input voltage.
- Main advantage is its high speed.
- Conversion time is NT
- The conversion time is independent of input voltage.
- The circuit is complex is one of its disadvantageous.

Advantageous:

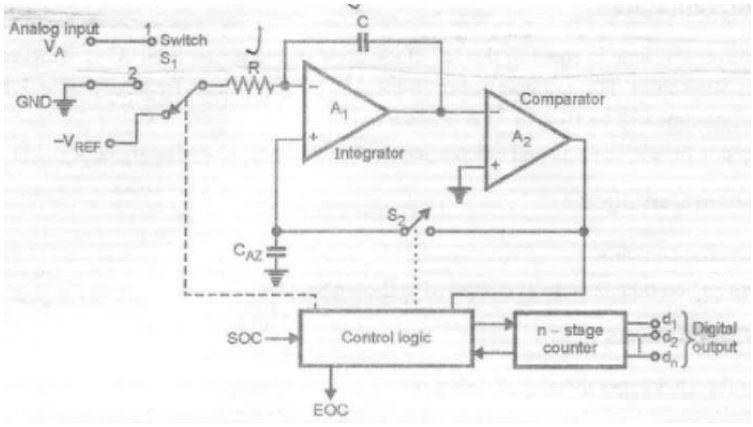
- Conversion time is very short and is independent of input voltage

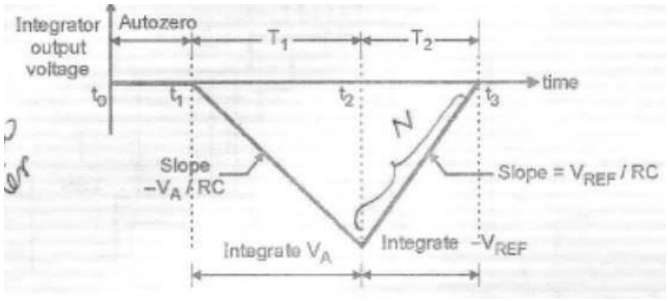
Disadvantageous:

- The circuit is complex
- The conversion time is more as compared to Flash type ADC.

UNIT – 5/ Lecture 9

Dual Slope Integrator ADC





- Conversion time $= 2^N T + nT$
- Maximum conversion time $= 2^{N+1}$
- Conversion time is independent of input voltage.

Advantageous:

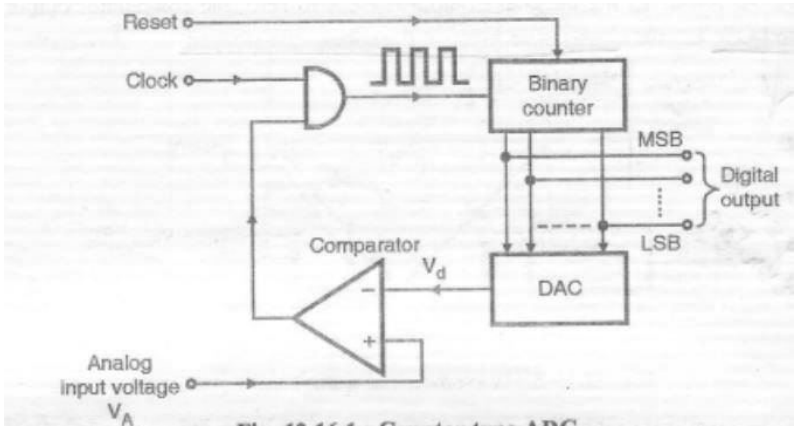
- Offset operations are used with relative easy use
- Low cost
- Accuracy of DS ADC can be 0.05% which is adequate for most applications.

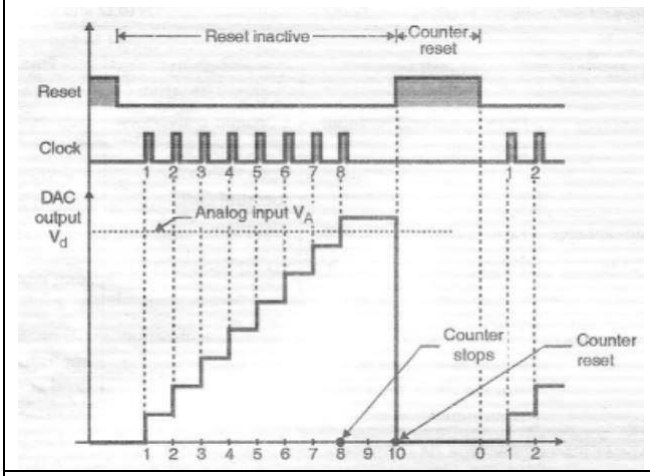
Disadvantages:

- Long conversion time as compared to other ADCs

UNIT – 5/ Lecture 10

Counter Type ADC





- Conversion Time = nT
- Maximum conversion time = $2^N T$
- Conversion time is function of input voltage

Advantages

- Simple construction
- Easy to design and less expensive
- Speed can be adjusted by adjusting the clock frequency
- It is faster than Dual Slope DAC.

Disadvantages

- The conversion time is function of input voltage

Example:

Figure shows a D to A converter. Find the output of Op Amp, if the input signal is 1011. Assume that binary 1 represents 5 V

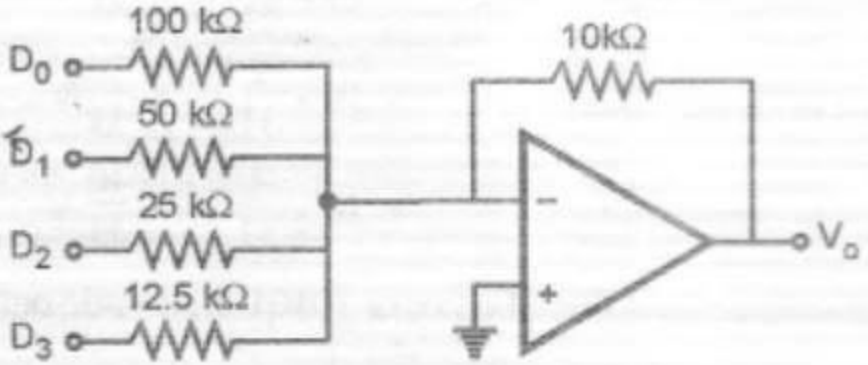


Fig. P. 12.22.1

$D_3\ D_2\ D_1\ D_0 = 1011,\ R_F = 10\ k\Omega,\ R = 12.5\ k\Omega$

V_o

$$V_o = V_R \cdot \frac{R_F}{R}\left[D_3\,2^0 + D_2\,2^{-1} + D_1\,2^{-2} + D_0\,2^{-3}\right]$$

$$= 5 \cdot \left(\frac{10}{12.5}\right)\left[1 + 0 + \frac{1}{4} + \frac{1}{8}\right] = 5.5\ V$$

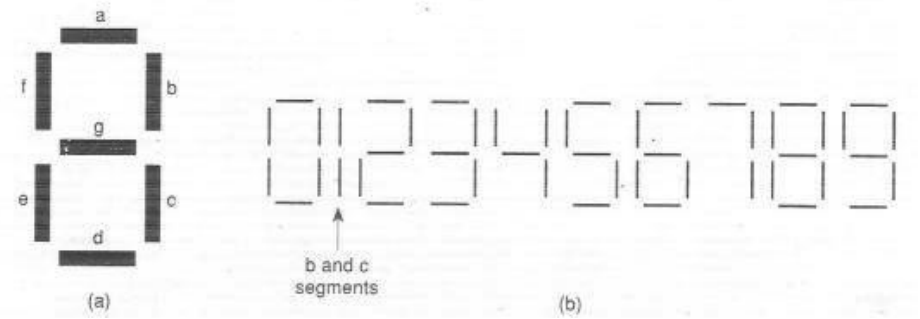
UNIT – 5

Clocks and Timing Circuits

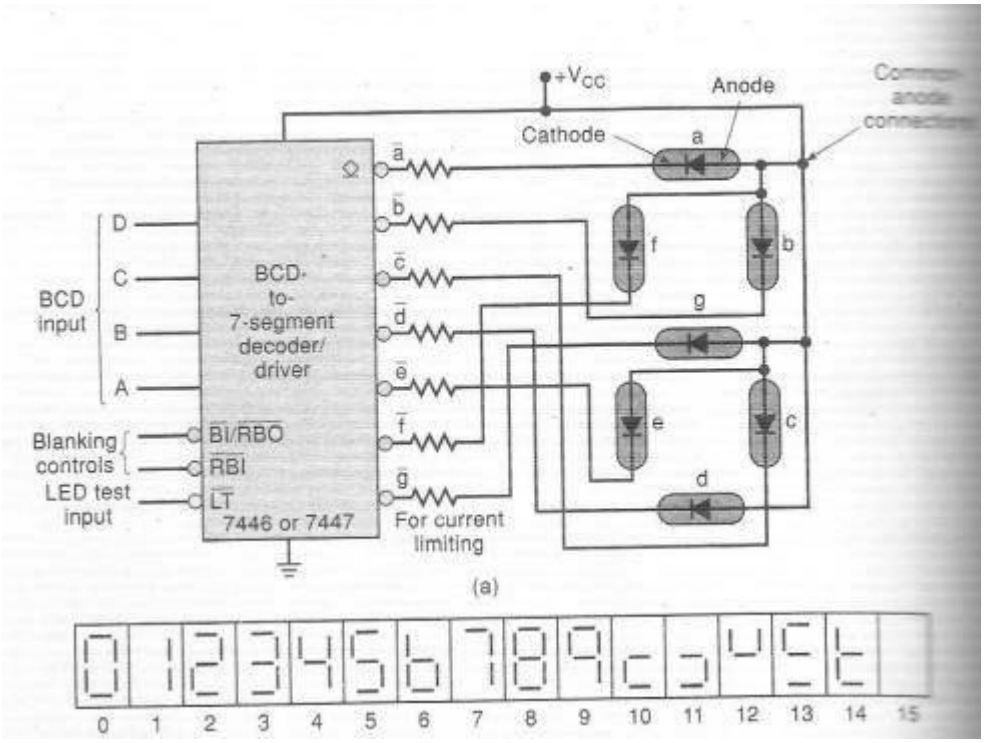
Unit-05/Lecture-11

7 Segment LED (Light Emitting Diode) Display

Contains segments from a to h



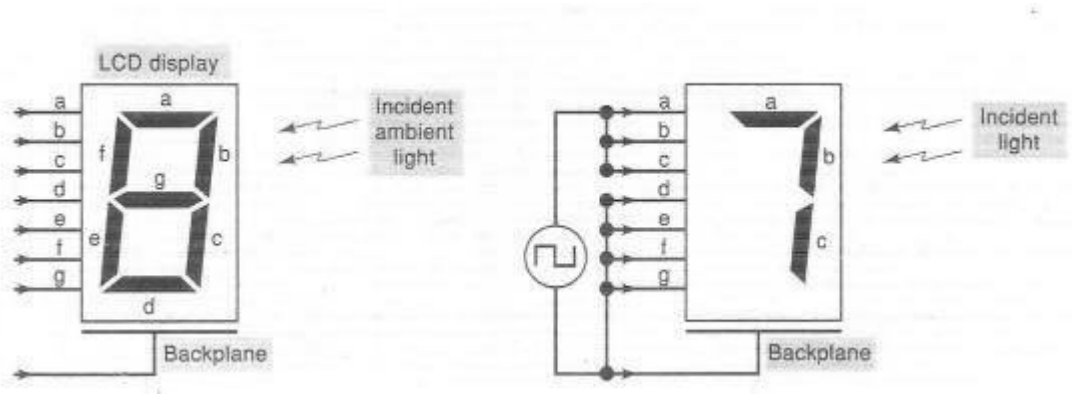
A BCD to 7 Segment used to drive the 7 Segments is as follows:



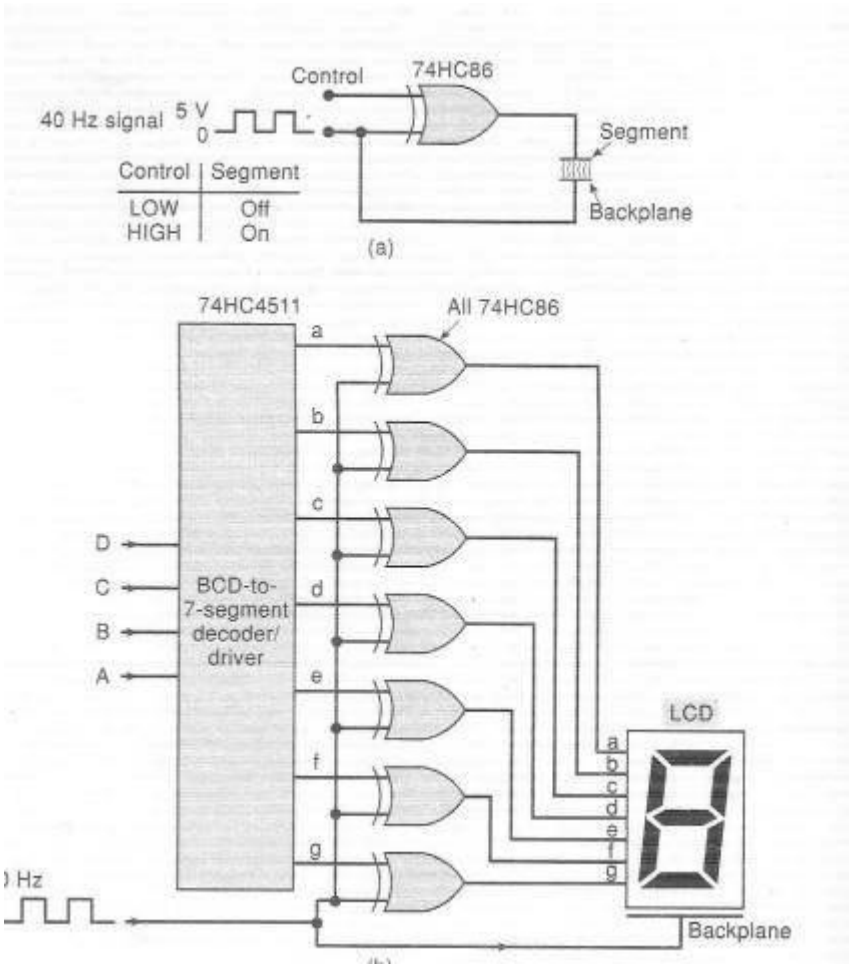
A corresponding low voltage at the output of the BCD i.e. at a to h will turn the diodeON and the resultant LED will glow to display the corresponding number.

LCD Displays

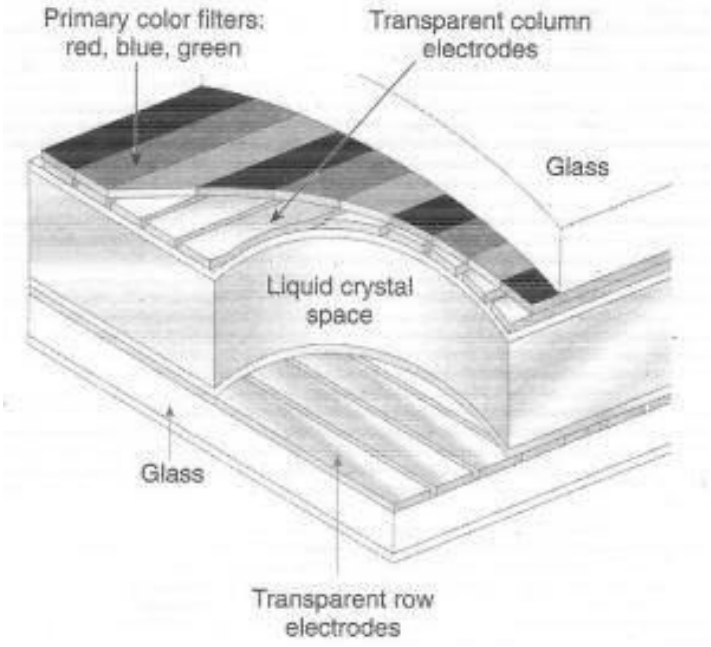
LCD basic arrangement and Applying voltage between the segment and the backpane turns ON the segment. Zero voltage turns the segment OFF. The molecules of the liquid filled inside will rotate to block or unblock the back lit LCD pane to unlit or light the front display.



Method of driving LCD segment and driving a 7 segment display



A passive panel LCD Matrix


Primary color filters:
red, blue, green
Transparent column
electrodes
Glass
Liquid crystal
space
Glass
Transparent row
electrodes