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MCSE - 103 M.E./M.Tech., I Semester

Examination, June 2014

Advanced Computer Architecture

Time: Three Hours

Maximum Marks: 70

Note: Attempt one question from each unit.

Unit - I

 a) The execution of an object code on a 400-MHz processor contains 2 × 10° instructions. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace;

Instruction	CPI	Instruction
type		mix
Arithmetic & logic	1	60° o
I oad store with cache hit	2	1800
Branch	4	12° o
Memory reference with		
cache miss	8](190

- Calculate the average CPI when the program is executed on a uniprocessor with above results.
- ii) Calculate the MIPS rate.
- b) Compare control flow data flow and reduction computers in terms of the program flow mechanism used

- 2. a) Explain flynn's classification of computer architecture.
 - b) Discuss the concept of Branch handling techniques and effect of branching and desire the performance degradation factor.

Unit - II

 a) Determine the data dependencies in the same and adjacent iterations of the given Do loop.

Do 10 j - L n

 $A(j+1) \cdot B(j-1) \cdot c(j)$

B(j) = A(j) + k

C(i) B(j) I

10 continue

- b) Explain internal data forwarding and possible hazards between read and write operations with respect to mechanism for instruction pipeline.
- 4. a) I xplain the implements two models of SIMD computers
 - Briefly explain how to overcome data hazards with dynamic scheduling using Tomasulo's approach.

Unit - III

- iii Differentiate between structural parallelism and instruction level parallelism
 - b) I xplain the search algorithm in parallel computing

- 6 a) Explain multiprocessing in MIMD mode and multiprocessing in MPMD mode.
 - b) Discuss the language features to exploit parallelism.

Unit - IV

- ". a) Discuss the multiprocessor scheduling strategies.
 - Explain process synchronization mechanism in multiprocessor environment.
- 8 a) Distinguish between synchronized parallel and asynchronous parallel algorithms.
 - b) Explain deadlock prevention and avoidance strategies in multiprocessing environment.

Unit - V

- 9 a) State and prove Amdalif's law
 - b) Define the following terms for various system interconnect architectures.
 - Node degree.
 - ii) Network diameter.
 - iii) Bisection bandwidth
 - iv) Symmelty in networks.

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- 10. Write short notes on the following
 - a). Scheduling and load balancing in multiprocessor
 - b) Vector processor
 - c). Cache coherence protocols
 - di. Slured memory multiprocessors