Roll No .....

MEDC-104

M.E./M.Tech. I Semester

Examination, December 2015

VLSI Design

Time : Three Hours

Maximum Marks : 70

Note : i) Attempt any five questions out of eight questions.
ii) All questions carry equal marks.
iii) Assume suitable data if required.

1. a) Explain the basic concept of integrated circuits and its manufacturing technologies. Discuss about any one technology in detail with the help of suitable example.
   b) Discuss about the fundamental design for digital CMOS circuits with the help of any one example.

2. a) Explain the terms "setup time" and "hold time" in relation to a CMOS D register. If a clock is delayed to a register with regard to the data input, which of these parameters varies and how?
   b) Discuss about the ECL and low voltage swing pads. Explain the similarity between the two.

3. a) Explain the design process which elaborates its capture, simulation and verification of any logic structure.
   b) Explain the memory and control strategies for subsystem design operations. Write an example.

4. a) Write short note on Semiconductor Memories. Explain the principle of SRAM and DRAM.
   b) Give a brief introduction about ROM analysis and design with the help of a suitable example.

5. a) Write an introductory note on Algotronix. Explain its CAL logic cell functions.
   b) Explain the concept of sea of gates and gate array design with example.

6. a) Discuss about the dissipated power. Write down its classification and explain them in brief.
   b) Explain the difference between programmable logic and programmable logic structures with the help of suitable structure.

7. a) Discuss about the CAD systems with its layout structure with a suitable example.
   b) Discuss the various testability issues facing during CAD implementation on MOS devices.

8. Write short note (Any two)
   a) Optimization
   b) Fault Tolerance
   c) Timing analysis
   d) Routing and Placement techniques

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