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Total No. of Questions :8] *[Total No. of Printed Pages :2*

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MEDC-104

M.E./M.Tech. I Semester

Examination, June 2017

VLSI Design

Time : Three Hours

Maximum Marks : 70

Note: i) Attempt any Five questions.
ii) All questions carry equal marks.
iii) Assume data where necessary.

1. a) What do you understand by design rules in CMOS? Explain in detail with suitable diagrams. 7
   b) Explain the integrated circuits production process and what are the methods of testing in detail. 7

2. a) Realize $Z = \overline{A(B+C)+DE}$ for clocked CMOS logic. 7
   b) Explain the difference between static and dynamic power in CMOS. 7

3. a) What do you understand by simulation which software proves to be suitable for the simulation in VLSI design. 7
   b) Summarize the differences between a 50G chip and a standard cell chip. What benefits does each implementation style have? 7

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4. a) A combinational circuit is to designed for squaring a given 3-bit number. Implement it using PLA and PROM. Give the truth table also. 7

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   b) How will you implement the ROM using sub-system design? Explain step by step. 7

5. Explain the methods of chip designing also explain the off-chip connectivity. Why is it so important? 14

6. a) Give the classification of memory with the application of each. 7
   b) What is the need of design for testability? With schematic explain different faults? 7

7. a) Explain static CMOS circuit design in detail. 7
   b) What is CAD system? Explain logic synthesis and simulation. 7

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8. Write short note on (any two): 14
   a) Body effect in CMOS.
   b) Channel length modulation in MOS.
   c) Ten step process for fabrication of MOS.
   d) Programmable gate array.

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