Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

MEDC-104

M.E./M.Tech., I Semester

Examination, November 2018

VLSI Design

Time : Three Hours

Maximum Marks : 70

Note: i) Attempt any Five questions.

ii) All questions carry equal marks.

1. a) What is Moore's Law? Explain its relevance with respect to evolution of IC technology. 7

   b) Explain VLSI design flow. 7

2. a) Design a CMOS equivalent circuit for 4 : 1 multiplexer. 7

   b) Write a short note on physical design. 7

3. a) Define simulation. With neat sketches explain the design flow of standard cell. 7

   b) Draw and explain the architecture of an FPGA with example. 7

4. a) Explain step by step sub system design approach with example. 7

   b) Compare the different types of CMOS subsystem multipliers. 7

5. Define placement. Write a short note on placement and routing. 14

6. Define the following terms

   a) Simulation and synthesis 7

   b) Various testability issues 7

7. a) Design a CMOS equivalent circuit for

   $F = \overline{(A + B)(C + D)}$ logic 7

   b) Design a CMOS equivalent circuit for $F = \overline{AB + CD}$ logic 7

8. a) With neat sketches explain the architecture of PLA. 8

   b) Define SPLD, CPLD and FPGA. 6

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