Total No. of Questions :8] *[Total No. of Printed Pages :2*

Roll No .....

MEVD-102

M.E./M.Tech. I Semester

Examination, June 2016

CMOS VLSI Design

Time : Three Hours

Maximum Marks: 70

Note : i) Attempt any five questions out of eight questions.
ii) All questions carry equal marks.
iii) Assume suitable data, if required.

1. a) Write an introductory note on VLSI Design flow. Explain the concept of design quality.

   b) Explain the second order effects. Draw and explain the sub threshold region.

2. a) Draw and explain the graphical derivation of CMOS inverter characteristic.

   b) Draw and explain the CMOS inverter noise margin. Explain its characteristics.

3. a) Explain the parasitic effects in Integrated circuits.

   b) Derive an expression for channel resistance in voltage current characteristics of MOS transistor.

4. a) Explain the concept of capacitance estimation in MOS systems.

   b) Draw and explain the accumulation, depletion and inversion function of V_{gs} in MOS capacitor characteristics.

5. a) What do you mean by Interconnect? Write and explain all circuit elements.

   b) Write down different design rules for layout circuit.

6. a) Explain the principle of Latch up. Discuss about its physical origin, its triggering and its prevention methods.

   b) Give an introductory note on CAD Tools. How this tool is beneficial for designing MOS circuits?

7. a) Discuss the designing of combinational logic parity generator.

   b) Write and explain different types of code generators.

8. a) Give an introductory note on dynamic register element. Give its applications also.

   b) Explain the designing of ALU subsystem. What is its significances in a circuit? Explain with a suitable example.

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