Total No. of Questions :8] *[Total No. of Printed Pages :2*

Roll No .....

MEVD - 103

M.E./M.Tech., I Semester

Examination, December 2015

Advanced Logic Design

Time : Three Hours

Maximum Marks : 70

Note : i) Attempt any five questions.
ii) All parts of each question are to be attempted at one place.
iii) All questions carry equal marks.

1. a) Implement the following logic function using three 2:1 multiplexers and one 2 input OR gate, assuming that variables, logic level high and logic level low are directly available as input:
   $F(A, B, C, D) = (A.B) + (B'.C) + D$
   b) Draw CMOS complex gate for the logic function:
   $F = XNOR (X, Y)$
   Use as few transistors as possible.

2. a) What is the difference between Wire and REG Data type?
   b) Explain about following operators of Verilog:
   i) Relational Operator
   ii) Bitwise Operator and Logical Operator
   iii) Conditional Operator
   iv) Shift Operator
   v) Concatenation Operator

3. a) Develop a Verilog model for a 7 segment decoder. Include an additional input "BLANK" that overrides the BCD input and causes all segments not to be lit.
   b) Implement a Verilog model for 4 bit Full Adder.

4. a) Write Verilog code for 74381 ALU Chip.
   b) Write Verilog Code for 2:1 MUX using if statement.

5. a) Design a sequence Detector which will generates z = '1' if the consecutive two zeroes or two ones comes at the input x. Form the state diagram.
   b) Write short notes on :
   i) Synthesis and simulation
   ii) Modelsim simulator

6. a) Write verilog code to implement the function:
   $f(x_1, x_2, x_3) = \Sigma m(0, 1, 3, 4, 5, 7)$
   using the continuous assignment.
   b) Write short notes on Verilog Data types.

7. a) Write code for Asynchronous reset D-Flip-Flop.
   b) Explain and differentiate Mealy type and Moore type finite state machines.

8. Explain the following terms:
   a) Metastability
   b) Noise margin
   c) Power dissipation
   d) Fan out
   e) Fan in

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