Total No. of Questions :8] *[Total No. of Printed Pages :3*

Roll No .....

MEVD - 203

M.E./M.Tech., II Semester

Examination, June 2014

VLSI Test and Testability

Time : Three Hours ***Maximum Marks : 70***

Note : i) Attempt any five questions.
ii) All questions carry equal marks.
iii) Assume the missing data, if any.

1. a) Explain the different types of faults and failure.

   b) Explain different levels of testing. Also discuss design for testability.

2. a) Explain why the (input or output) inertial delay of a gate cannot be greater than the smallest transport delay associated with the gate i.e. $d_I \leq \min \{d_r, d_f\}$ where d_I is inertial delay, d_r is rise delay and d_f is fall delay.

   b) For the circuit of figure 1

      i) Find the set of all tests that defects the fault C s-a-1.

      ii) Find the set of all tests that detect the fault a s-a-0.

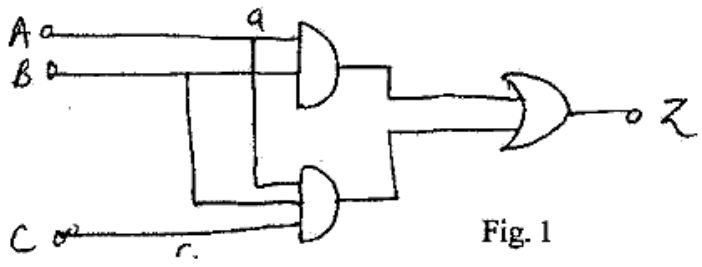

Fig. 1

3. a) Prove that in a combinational circuit if two faults dominate each other, then they are functionally equivalent.

   b) For the circuit of figure 2.

      i) Find the set of all tests that detect the fault b s-a-1.

      ii) Find the set of all tests that distinguish the fault a s-a-0 and d s-a-0.

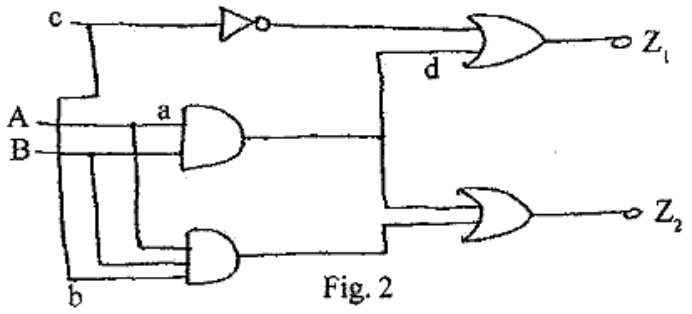

Fig. 2

4. a) Design a ALFSR for the following polynomial. Also find out the generated number sequence by the ALFSR. $P(x) = x^4 + x^3 + 1$.

   b) Design a synchronous sequential circuit for the state table given in following table using the scan path design method and design a test sequence.

Present State	Input N.S./ Output	
	$X = 0$	$X = 1$
A	A/0	B/0
B	A/0	B/1
C	D/1	C/1
D	C/0	A/0

5. a) Explain the testing of sequential circuit as iterative combinational circuit.

   b) Explain the D-algorithm for test generation. Also explain the working of D-algorithm using an example.

6. a) Explain the IEEE standard 1149.1 for board and system-level boundary scan. Also discuss the boundary scan cell.

   b) Explain Ad-Hoc testable design techniques.

7. a) For a two-input AND gate and a two-input exclusive-OR gate, develop the singular cover of the gates the propagation D-cubes and primitive D-cubes of failure for a s-a-1 fault on one of the gate inputs.

   b) Discuss the generic offline BIST architecture.

8. Write a short note on following (any four)

   i) Controllability and Observability

   ii) Reliability

   iii) IDDQ testing

   iv) Fault collapsing

   v) RAM BIST

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