

MEVD - 203**M.E./M.Tech., II Semester**

Examination, July 2015

VLSI Test and Testability*Time : Three Hours**Maximum Marks : 70*

- Note :** i) Attempt any five questions.
 ii) All questions carry equal marks.
 iii) Assume the missing data, if any.

1. a) Discuss the different types of testing with the help of different criterion and attributes of testing method.
 b) What is stuck at faults? How do you model them?
2. a) Explain event driven simulation with the help of neat flow chart.
 b) Show that the two faults $C/s-a-0$ and $f/s-a-1$ are equivalent in the circuit of figure 1.

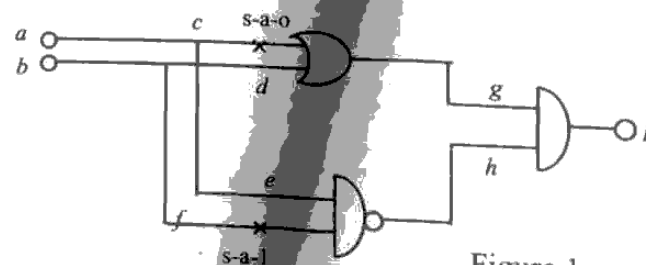


Figure 1

3. a) Prove that in a combinational circuit if two faults dominate each other, then they are functionally equivalent.
- b) Determine the output function of the circuit of figure 2 for the following faults.
- AND bridge between inputs of Gate G1.
 - The multiple fault (x_3 s-a-1, x_2 s-a-0)

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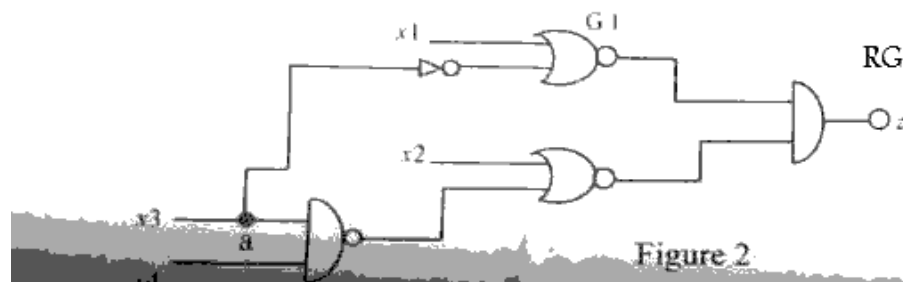


Figure 2

4. a) Discuss the Path Oriental Decision Making (PODEM) algorithm to generate a test for combinational circuit with the help of flow chart.
- b) Find a test for detecting a fault 6 s-a-0 in the circuit shown in figure 3 using D-algorithm.

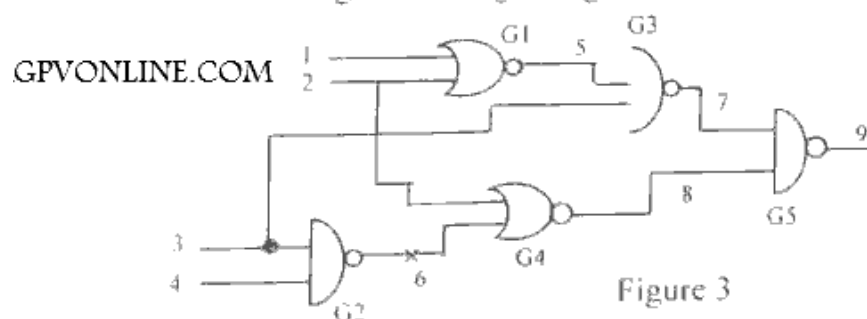


Figure 3

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5. Design a Built In Logic Block Observer (BILBO) with following operating mode. Also draw the block diagram of BILBO to test CLB.

B1	B2	Input-mux	D	Function	Test function
0	0	Scan-In	li	Parallel load Register	Normal (non test) mode
0	1	Scan-In	Fi-1	Linear shift Register	Scan path mode
1	0	Feedback	li	MISR	Signature analysis
1	1	Feedback	-	ALFSR	Pattern Generation for testing

6. a) Describe full and partial scan design for sequential circuit.
- b) Explain the boundary scan cell.
7. a) Discuss the generic offline BIST architecture.
- b) Explain how test point insertion will improve random testability in BIST architecture.
8. Write short notes on following (any four)
- Aliasing
 - PI A testing
 - Controllability and observability
 - Reliability
 - Boolean difference method.

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