Total No. of Questions :8] *[Total No. of Printed Pages :2*

Roll No .....

MEVD-203

M.E./M.Tech., II Semester

Examination, December 2016

VLSI Test and Testability

Time : Three Hours

Maximum Marks : 70

Note : i) Attempt any five questions out of eight questions.
ii) All questions carry equal marks.
iii) Assume suitable data, if required.

1. a) Explain the concept of testing in VLSI circuit with the help of suitable example.
   b) Give a brief exposure in CMOS testing techniques. Write and explain any one technique.

2. a) How many types of faults are there in VLSI system? Give a brief classification. Explain each of them with the help of suitable example.
   b) Define "Elementary concepts". Why is it important and prime factor in CMOS testing?

3. a) What do you mean by delay models? Explain the concept of event driven simulation with example.
   b) Give a brief note on stuck at faults. Explain its types with the help of a suitable example.

4. a) Write an example explaining full scan and partial scan designs.
   b) Explain D-Algorithm with example.

5. a) Write an introductory note on automatic test pattern generator.
   b) Write an example which used to test sequential circuits for the iterative combinational circuits.

6. a) Explain Ad-hoc testing method. Give a comparison between full and partial scan design .
   b) Write a logic equation explaining the logic BIST random pattern for testability factor.

7. a) Explain IDDQ testing. Also, discuss about the IDDQ test patterns.
   b) Explain any suitable design parameters for IDDQ testability patterns.

8. Write short notes (any four) :
   a) RAMBIST
   b) Fault collapsing
   c) Boundary scans
   d) PODEM
   e) Response analyzers

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