Total No. of Questions : 8] *[Total No. of Printed Pages : 2*

Roll No .....

MEVD-203

M.E./M.Tech. II Semester

Examination, June 2017

VLSI Test & Testability

Time : Three Hours

Maximum Marks : 70

Note: i) Attempt any five questions out of eight questions.
ii) All questions carry equal marks.
iii) Assume suitable data, if required.

1. a) Explain the concept of failures and faults in CMOS testing design functions.
   b) Give a brief exposure in CMOS testing levels. Discuss about the test economic.

2. a) What are the basic differences between system and field testing? Explain it with suitable examples.
   b) Define "elementary concepts". Why is it in portant and prime factor in CMOS testing?

3. a) What do you mean by event driven simulation process? Explain the concept with example.
   b) Give a brief note on stuck at faults. Explain its types with the help of a suitable example.

4. a) Write an example explaining fault detection using Boolean Difference.
   b) Explain D-Algorithm with example.

5. a) Write an introductory note on automatic test pattern generator.
   b) Explain the differences between the primitive and propagation cubes.

6. a) Explain the concept of testing of sequential circuits as iterative combinational circuits.
   b) Explain with the suitable example for weighted random pattern testability.

7. a) Explain IDDQ testing. Also, discuss about the IDDQ test patterns.
   b) Explain any suitable design parameters for IDDQ testability patterns.

8. Write short notes (any four)
   a) SPOOF
   b) BIST architecture
   c) Boundry Scans
   d) PODEM
   e) Response analysers

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