MEVD-102

M.E./M.Tech. (First Semester)

EXAMINATION, Dec 2010

(Grading/Non-Grading)

CMOS VLSI DESIGN

Time: Three Hours

Maximum Marks: GS:70

Note: Attempt any two parts from each question.

1. (a) Define abstraction level. Explain Gajeski's Y-chart. What is its significance in VLSI design?
   (b) Give the VLSI design flow and explain it.
   (c) What are frontend and backend tools? Explain with suitable examples. Why EDA tools are required for VLSI design?

2. (a) Discuss various types of power dissipation in CMOS circuits. Suggest some methods to minimize power dissipation.
   (b) Describe parasitic effect in integrated circuits with suitable example.
   (c) Explain CMOS logic structures and clocking strategies.

3. (a) Explain wafer preparation and its cleaning polishing for VLSI devices.
   (b) What is CMOS latch problem and how it is avoided? What is bird's beak enchrochment?
   (c) Explain layout design rules and technology related CAD issues.

4. (a) Explain the working of CMOS inverter. Illustrate VTC and explain each region of operation.
   (b) Describe subsystem design process and design of full adder.
   (c) Discuss design of ALU subsystem and dynamic shift register.

5. (a) Describe evolution of programmable logic devices with example.
   (b) Explain computer aided design flow for FPDs.
   (c) Discuss about the following:

   i. SPLDs
   ii. CPLDs and FPGAs