EC – 606 Software Lab- IV

VHDL

Hardware abstraction, Basic language elements: identifiers, data objects, data types, operators, behavioral modeling, data flow modeling, structural modeling, simulation and analysis.

VERILOG

Overview of digital design with Verilog, Hierarchical Modeling: basic concepts, models and ports, gate level modeling, data flow modeling, behavioral modeling, logic synthesis with Verilog HDL, simulation.

Experiments:

Design and simulation of following using Verilog/ VHDL . Logic gates: NAND, NOR, XOR, XNOR. Half adder, full adder, subtractor, latches, multiplexers- 2:1, 4:1, 8:1, comparators, decoders- 2:4, 3:8, 4:16. 4-bit ripple carry full adder,4-bit Ripple carry counter, parity generator, up/down counters.

References:

1. Samir palnitkar: Verilog HDL- A Guide to Digital Design and Synthesis, Pearson Education.
2. Bhasker: A Verilog HDL Primer –synthesis, Pearson Education
3. Pedroni: Circuit Design with VHDL, PHI Learning.
4. Perry: VHDL- Programming by example, TMH.